Ms. Preeti Goyal

Designation: Assistant Professor
Qualification: Ph.D (Purs.), M.Tech, BE
Specialization: VLSI Design
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Education

Ph.D. (Pursuing) "**Modelling, Simulation and Analysis of TFET for Analog and RF applications**" from GGSIPU, Delhi.

Masters in VLSI Design (Electronics and Communication Engineering Department) from CDAC Noida, GGSIPU, 2005-2007.

BE in Electronics and Communication Engineering from MDU, 2001-2005.

Research Interest

VLSI Design, Embedded System Design.

Publications

International Journals: 01
National Journals: 01
International Conferences: 02

List of Publications

[1]. Preeti Goyal, Jaya Madan, Garima Srivastava, Rahul Pandey, and R. S. Gupta. "Performance Analysis of Drain Pocket Hetero Gate Dielectric DG-TFET: Solution for Ambipolar Conduction and Enhanced Drive Current." *Silicon* (2022): 1-11.

[2]. Preeti Goyal, Tanvi Agrawal, Arti Noor and Sunita Prasad "Area Efficient FPGA Implementation of AES-128" IUP Journal of Science and Technology, Sep 2008, Vol 4 Issue 3, P17.

[3]. Preeti Goyal, Garima Srivastava, Sonam Rewari, and R. S. Gupta. "Controlling Ambipolarity and Rising Ion in TFETs for Enhanced Reliability: A Review." In *2020 5th IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE)*, pp. 1-6. IEEE, 2020.

[4]. Preeti Goyal, Garima Srivastava, Jaya Madan, Rahul Pandey, and R. S. Gupta. "Source Material-Engineered Charge Plasma based Double Gate TFET for Analog/RF Applications." In *2021 International Conference on Industrial Electronics Research and Applications (ICIERA)*, pp. 1-4. IEEE, 2021.