Dr. Anubha Goel

Assistant Professor, Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology.

Phone: +91-9968058820
Email: anubhagoel15@gmail.com
Orcid ID: https://orcid.org/0000-0002-0400-5664
Office Address: Room No. 432, 4th Block, Maharaja Agrasen Institute of Technology, PSP Area, Plot No. 1, Sector-22, Rohini, New Delhi-110086.

SUMMARY

- Working as an active member of various committees for NBA accreditation at **Maharaja Agrasen Institute of Technology**.
- Working as an active member of the organizing committee for cultural events at **Maharaja Agrasen Institute of Technology**.
- Had been awarded a **special increment** for **extraordinary efforts in teaching** during probation period at **Maharaja Agrasen Institute of Technology**.
- Around 12 Years of experience in academics as an Assistant Professor.
- Around 12 months of experience in the field of Product Validation.
- Team Worker with good interpersonal and fast learning skills.
- A dynamic and hardworking go-getter with abilities to accept challenges and deliver results.
- Excellent communication and presentation skills.
- Ability to handle many concurrent tasks & do them all with excellence.

PROFESSIONAL EXPERIENCE

- Presently working as an **Assistant Professor** in **Maharaja Agrasen Institute of Technology** (affiliated to GGSIPU) as a part of Electronics and communication department (Jan, 2009 to till date)
- Worked as a **Product Validation Engineer** with **Calypto Design Systems**, Noida (October 2007 to October 2008) on the project "Product Validation for SLEC" (**M.Tech Thesis**)

ACADEMIC RECORD

- **Ph.D (VLSI Design)**, **2021**, titled: "Modeling, Simulation and Characterization of Different Surrounding Gate (SG) MOSFET Architectures for GIDL Reduction and High Frequency Applications" from **Banasthali Vidyapith**, Rajasthan(with **1 patent, 7 SCI Journals (2 IEEE Publications), 5 copyrights**).
- **M.Tech (VLSI Design)**, **2008**, from **Banasthali Vidyapith**, Rajasthan **77.75 %** (**Second Topper**).
- **B.Tech (Electronics & Communication), 2006**, from **Maharaja Agrasen Institute of Technology,** Rohini (**GGSIPU** University, Delhi), **78.88% (Second Topper)**
- **Diploma (Electronics with Specialization in Digital Electronics and Micro-processor System Design), 2003** from **Kasturba Polytechnic for Women**, **BTTE**, Delhi, **75%**
- **10th , 2001**, from **Ramjas School, Pusa Road**, New Delhi, **87%**
- Worked as a **Research Assistant**, in a **Live Project** "**Automatic Battery Monitoring System**" sponsored by **Exide Batteries** at **Banasthali Vidyapith.**
- **Second prize** in Electronics Model Making Competition, at University Level, held at **Guru Gobind Singh Indraprastha University**, Delhi, for **Automatic Multi-Storey Car Parking System.**
- Worked as a Lab Professor in the **Auburn University** for the subject "**Digital Electronics**" and "**Digital Circuits and Systems**".

AREA OF EXPERTISE

VLSI Design, Semiconductors, Device Modelling

RESEARCH PUBLICATIONS

I. ***Papers in Reviewed Journal (Published)***

1. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, "Temperature-dependent gate-induced drain leakages assessment of dual-metal nanowire field-effect transistor—analytical model" **IEEE Transactions on Electron Devices,** Volume: 66, Issue: 5 , pp 2437 – 2445, May 2019. (Print ISSN: 0018-9383 Online ISSN: 1557-9646 Digital Object Identifier 10.1109/TED.2019.2898444, Impact Factor: 2.62).

2. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, "Shallow Extension Engineered Dual Material Surrounding Gate (SEE-DM-SG) MOSFET for Improved Gate Leakages, Analysis of Circuit and Noise Performance," **AEU-International Journal of Electronics and Communications (Elsevier)**, Volume: 111, pp 152924, Nov 2019. (Print ISSN: Online ISSN: 1434-8411 Digital Object Identifier: 10.1016/j.aeue.2019.152924, Impact Factor: 2.924).

3. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, " High-K Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGS-JGAA) MOSFET for High Frequency Applications, " **Microsystem Technologies Journal (Springer)**, Volume: 26, Issue: 5, pp 1697-1705, Dec 2019. (Print ISSN: 0946-7076 Online ISSN: 1432-1858; Digital Object Identifier: 10.1007/s00542-019-04715-6, Impact Factor: 1.513).

4. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, "Modeling of Shallow Extension Engineered-Dual Metal-Surrounding Gate (SEE-DM-SG) MOSFET- Gate Induced Drain Leakages (GIDL)," **Indian Journal of Physics (Springer)**, Volume: 5, pp 1-10, March 2020. (Online ISSN: 0946-7076, Digital Object Identifier: 10.1007/s12648-020-01704-8, Impact Factor: 1.242).

5. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, "Physics based Analytic Modeling and Simulation of Gate-Induced-Drain-Leakage and Linearity Assessment in Dual-Metal Junctionless Accumulation Nano-Tube FET (DM-JAM-TFET)," **Applied Physics A (Springer)**, Volume:126, pp. 1-4, May 2020. (Print ISSN: 0947-8396, Online ISSN: 1432-0630, Digital Object Identifier: https://doi.org/10.1007/s00339-020-03520-7, Impact Factor: 1.784).

6. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, "Novel Dual-Metal Junctionless Nanotube FET (DMJN-TFET) for Improved Analog and Low Noise Applications," **Journal of Electronic Materials (Springer)**, vol. 50, pp.: 108-119, 2021. (Print ISSN: 0361-5235, Digital Object Identifier: 10.1007/s11664-020-08541-9, Impact Factor: 1.774). **[SCI JOURNAL]**

7. **Anubha Goel,** Sonam Rewari, Seema Verma, S. S. Deswal and R.S. Gupta, "Dielectric Modulated Junctionless Biotube FET (DM-JL-BT-FET) Bio-Sensor," **IEEE Sensors Journal**, vol. 21, no. 15, pp. 16731-16743, 1 Aug.1, 2021. (Print ISSN: 1530-437X, Online ISSN: 1558-1748, Digital Object Identifier: 10.1109/JSEN.2021.3077540, Impact Factor: 3.076).

8. Swati Sharma, **Anubha Goel**, Sonam Rewari, Vandana Nath and R. S. Gupta "Enhanced Analog Performance and High-Frequency Applications of Dielectric Engineered High-K Schottky Nanowire FET," **Silicon-Springer** (Accepted), vol. , no. , pp. , 2022. (Print ISSN: 1876-990X, Online ISSN: 1876-9918, Digital Object Identifier: 10.1007/s12633-022-01663-1, Impact Factor: 2.670).

9. Neeraj, **Anubha Goel**, Shobha Sharma, Sonam Rewari & R. S. Gupta. "SiC Based Analytical model for Gate - Stack Dual Metal (DM) Nanowire FET with Enhanced Analog Performance**" International Journal of Numerical Modelling: Electronic Networks, Devices and Fields-John Wiley and Sons, Ltd,** Jan 2022 (Accepted), vol. , no. , pp. , 2022. (Online ISSN: 1099-1204, Digital Object Identifier: http://doi.org/10.1002/jnm.2986, Impact Factor: 1.296).

II. ***Papers in International Conference (Published)***

[1] *"Shallow Extension Engineered Dual Metal Surrounding Gate (SEE-DM-SG) MOSFET for lower leakages and Submillimeter Wave Applications",* Anubha Goel, Sonam Rewari, Seema Verma and R.S.Gupta, 12th INDIACom; 2018 5th IEEE International Conference on Computing for Sustainable Global Development, BVICAM, 14-16 March, 2018, New Delhi, India.(ISSN: 0973-7529 ISBN: 978-93-80544-28-1)

[2] **"***Impact of Shallow Extension Engineering (SEE) on Analog and Digital Performance of Surrounding Gate (SG) MOSFET for High Frequency, High Gain and High Speed Real Time Applications",* Anubha Goel, Sonam Rewari, Seema Verma and R.S.Gupta, Micro2018; 5th International Conference on Microelectronics, Circuits & Systems, Applied Computer Technology, May, 19th - 20th , 2018, Bhubaneswar, Odisha, India.(ISBN: 81-85824-46-1)

[3] *"Dielectric Modulated Triple Metal Gate All Around MOSFET (TMGAA) for DNA Bio-Molecule Detection",* Anubha Goel, Sonam Rewari, Seema Verma and R.S.Gupta, 2018 IEEE Electron Device Kolkata Conference (2018 IEEE EDKCON), The Pride Hotel, Kolkata, 24-25 November, 2018, Organized by IEEE EDS Kolkata Chapter, EDKCON 2018, Kolkata, India.(ISBN: 978-1-5386-6415-5)

[4] "*High-K Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGSU-JGAA) MOSFET for High Frequency Applications",* Anubha Goel, Sonam Rewari, Seema Verma and R.S.Gupta, 8th International conference ; CCSN-2019 on "Computing, Communication and Sensor Networks", held during 19-20 Oct, 2019 in Institute of Aeronautical Engineering, Hyderabad, Telengana, India.(ISBN:81-85824-5)

[5] *"Dual-Metal Junctionless Nanotube FET (DMJN-FET) for Improved Analog Applications",* Anubha Goel, Sonam Rewari, Seema Verma and R.S.Gupta, 8th International conference ; CCSN-2019 on "Computing, Communication and Sensor Networks", held during 19-20 Oct, 2019 in Institute of Aeronautical Engineering, Hyderabad, Telengana, India.(ISBN: 81-85824-5)

[6] ***"****GaN Based Dual-Metal Gate Stack Engineered Junctionless-Surrounding-Gate (DMSEJSG) MOSFET for High Power Applications",* Anubha Goel, Sonam Rewari, Seema Verma and R.S.Gupta, 16th IEEE India Council International Conference; Indicon-2019 on "Applying Artificial Intelligence in Engineering for Prosperity and Betterment of Humanity", held during 13-15 Dec, 2019 in Marwadi University, Rajkot, Gujarat, India. (ISBN: 978-1-7281-2327-1)

[7] ***"****Gate - Stack Dual Metal (DM) Nanowire FET with Enhanced Analog Performance for High Frequency Applications",* Neeraj, Shobha Sharma, Anubha Goel, Sonam Rewari, R.S.Gupta, 4th International Conference, organized by IEEE EDS KGEC Student Branch Chapter; DevIC-2021 on "2021 Devices for Integrated Circuits", held during 19-20 May, 2021 in Kalyani Government Engineering College (Online Mode Conference), India. (ISBN: 978-1-7281-9955-9, pp. 373-377, Digital Object Identifier: 10.1109/DevIC50843.2021.9455919).

[8] ***"****Gallium Nitride Cylindrical Schottky Barrier MOSFET(GaN-CSB-MOSFET) For High - Frequency Implementation",* Swati Sharma, Anubha Goel, Sonam Rewari, Vandana Nath and R. S. Gupta, IEEE International Conference on Industrial Electronics Research and Application (ICIERA 2021), organized by Maharaja Agrasen Institute of Technology, held during 22-24 Dec, 2021 in Maharaja Agrasen Institute of Technology (Hybrid Mode Conference), India. (ISBN: , pp. , Digital Object Identifier:).

V. ***Poster Presentation in International Conference***

[1] *"Linearity and Intermodulation Distortion Assessment of Underlap Engineered Cylindrical Junctionless Surrounding Gate MOSFET for Low Noise CMOS RFIC Design",* Anubha Goel, Sonam Rewari, Seema Verma and R.S.Gupta, International Conference; Indicon-2019 on "Applying Artificial Intelligence in Engineering for Prosperity and Betterment of Humanity", held during 13-15 Dec, 2019 in Marwadi University, Rajkot, Gujarat, India. (ISBN: 978-1-7281-2327-1)

III. ***Copyrights (Registered)***

1. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, Diary No.: 5085/2020-CO/SW, titled "Dual-Metal Junctionless Accumulation Mode Overlap MOSFET for High Frequency Applications", dated March 18, 2020, ROC No.: SW-13633/2020.

2. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, Diary No.: 5098/2020-CO/SW, titled "Dual-Metal Junctionless Nanotube FET", dated March 18, 2020, ROC No.: SW-13632/2020.

3. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, Diary No.: 5101/2020-CO/SW, titled "Triple-Metal Gate All Around Based Bio-Sensor", dated March 18, 2020, ROC No.: SW-13641/2020.

4. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, Diary No.: 5103/2020-CO/SW, titled "Nanotube MOSFET based Bio-Sensor", dated March 18, 2020, ROC No.: SW-13543/2020.

5. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, Diary No.: 1825/2020-CO/SW, titled "Temperature Dependent Gate Induced Drain Leakage Assessment using Dual Metal Nanowire Field Effect Transistor", dated Jan 30, 2020, ROC No.: SW-13878/2020.

IV. ***Patent (Granted)***

1. **Anubha Goel,** Sonam Rewari, Seema Verma and R.S. Gupta, Patent application with application number-**201911025496,** titled "A Nanotube BIOSENSOR for DNA and Biomolecule Detection ", dated June 26, 2019.