

## Bio-Data of Professor R.S. Gupta

1.

**Name** Prof. R.S. Gupta

*Designation* **Professor**

*Department Institute and Address* Department of Electronics and Communication  
Maharaja Agrasen Institute of Technology  
Sector-22, Rohini,  
Delhi-110086

Mobile: 9810458959

E-mail: [rsgupta1943@gmail.com](mailto:rsgupta1943@gmail.com)

January 10, 1943

*Date of Birth*

2.

*Educational Qualifications*

- B.Sc. (Physics, Chemistry, Maths) Agra University, 1963.
- M.Sc. Physics (Electronics) Agra University, 1966.
- Ph.D. (Electronics Engineering) Institute of Technology, Banaras Hindu University, 1970 on *Study of the Amplifier Characteristics and Stability of Composite Transistors*.

*Courses on:*

- Course on *VLSI Technology and Design*, Sponsored by Ministry of Education, IIT, Delhi 1984.
- Course on *Microelectronics Technology and Design Programme*, Sponsored by Ministry of Education, IIT, Delhi, 1984
- Course on *Phased Array Radar Technology*, IIT, Delhi, February 9-11, 1995.

3.

*Membership of professional organizations*

1.	<b>Life Senior Member IEEE</b> – SM 07132517.
2.	<b>Life Fellow (LF)</b> – The Institution of Electronics and Telecommunication Engineers – F-023099
3.	<b>Member</b> – India Chapter ICTP (Italy)
4	<b>Life Member</b> – Semiconductor Society (India).

5.	<b>Chairman</b> – Society for Microelectronics and VLSI
6.	<b>Chairman</b> – IEEE-EDS Delhi Chapter (2007-2011)
7.	Member IEEE EDS Delhi Chapter 2012- continued

#### 4. Teaching & Research Experience

Name of Institution	Position	From	To	Total Experience
<b>Maharaja Agrasen Institute of Technology</b>	<i>Professor</i>	May 1, 2010	Till date	--
<b>University of Delhi</b>	<i>Emeritus Scientist (CSIR)</i>	May 2008	May 2009	1 year
<b>University of Delhi</b>	<i>Professor</i>	Nov. 19, 1997	Jan. 9, 2008	12 years
	<i>Reader</i>	Nov. 19, 1987	Nov. 18, 1997	10 years
<b>Ramjas College</b>	<i>Lecturer in Reader grade</i>	Jan. 1, 1986	Nov. 18, 1987	1 years 11 months
<b>-do-</b>	<i>Lecturer</i>	Aug. 27, 1971	Dec. 31, 1985	14 years 4 months
<b>Institute of Technology Banaras Hindu University</b>	<i>Part time lecturer &amp; research fellow</i>	Dec. 1, 1967	Aug. 26, 1971	3 years 9 months
<b>V.S.S.D. College, Kanpur</b>	<i>Lecturer</i>	Aug. 1, 1967	Nov. 30, 1967	4 months
<b>S.K.K. College, Etawah</b>	<i>Lecturer</i>	August 1966	July 31, 1967	1 year

#### 5. Research Specialization

**Solid State Electronics Devices, VLSI Design and modeling of Microelectronic Devices (MOSFET, MESFET, HEMT)**

#### 6. Research work done in this or related area in the past

Engaged in the analytical modeling, design and characterization of micron and submicron MESFET, MOSFET and HEMT devices. The thrust of the work has been on the development of useful models with different profiles and their electrical characterization. The work has resulted in more than 650 publications in various international/national journals and International & National Conferences. The work is well recognized among the leading groups in the field and summarized below. Also 39 students have got their Ph.D. degrees under his guidance. In addition he has supervised more than 16 students. At present he is supervising 6 students.

## **7. Conferences/Workshop organized Under IEEE activities**

1. Professor Vijay K. Arora, from Division of Engineering, Wilkes University, Wilkes-Barre, PA 18766, USA gave an *IEEE EDS Distinguished Lecture* on “Quantum Nano-Engineering-Quantum and High Field Nanoelectronics Transport” on February 20, 2009.
2. Professor Albert Wang, Fellow-IEEE, Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521, USA, gave an *IEEE EDS Distinguished Lecture* on “ESD Protection Design for RF/AMS ICs” on May 29, 2009 at Department of Electronic Science, University of Delhi South Campus, New Delhi, India
3. Mini-Colloquia on "Compact Modeling of advance MOSFET structures and mixed mode applications" at University of Delhi South Campus, New Delhi, India sponsored by the IEEE Electron Device Society under its Distinguished Lecturer Program on January 5-6, 2008.
4. IEEE-Distinguished Lecturer talks by Dr. M.K. Radhakrishanan (EDS Chapter Partner & Point of Contact for EDS Chapters in South-Asia), Title of the talk - "Nanoelectronic Devices – Analysis Challenges", on 9<sup>th</sup> February 2008.
5. IEEE-Distinguished Lecturer talks on 5<sup>th</sup> & 6<sup>th</sup> January 2008.
6. IEEE-Distinguished Lecturer talks by Prof. Vijay K. Arora from Division of Engineering, Wilkes University, Wilkes-Barre, USA, The title of talk is “Failure of Ohm's Law: Its Implications on the Design of Nanoelectronic Devices and Circuits”, November 5, 2007.
7. IEEE-Distinguished Lecturer talks by Dr. Ashok K. Kapoor, TSMC, Title of the Talk “Growth of Semiconductor Technology driven by the needs of information Technology”, July 9, 2007
8. Robotics tutorial programmes by apple satellite 1983 organised.
9. Annual convention and exhibition – 1981 organised.
10. Workshop on magnetic materials – 1981 organised.
11. Workshop on advances in microwave circuit design on 1980 applications organised.
12. Workshop on remote setting techniques organised and applications – 1979 (IEEE-ED).
13. Workshop on design measurement & evaluation of microwave atoms systems – 1978 organised (IEEE-ED).
14. Measurement and evaluation of microwave system in 1977 organised (The Institute of Electrical and Electronics Engineers Inc., USA).

INTERNATIONAL

1. **Chairman** *12th International Symposium on Microwave and Optical Technology (ISMOT-2009)* to be held in Ashoka Hotel from December 16 – 19, 2009.
2. **Chairman** *16<sup>th</sup> Asia-Pacific Microwave Conference (APMC '04)*, University of Delhi, to be organized in Dec. 15-18, New Delhi, 2004.
- 3.(i) **Secretary** *8<sup>th</sup> Asia-Pacific Microwave Conference (APMC '96)*, University of Delhi, Dec. 17- 20, Hotel Ashok, New Delhi, 1996.
- (ii) **Chairman: Technical Program** *8<sup>th</sup> Asia-Pacific Microwave Conference (APMC'96)*, University of Delhi, December 17 - 20, Hotel Ashok, New Delhi, 1996.
4. **International Steering Committee member** *Asia-Pacific Microwave Conference (APMC-2005)*, Suzhou, China, December 4-7, 2005.
5. **Secretary** *International Symposium on Recent Advances in Microwave Technology (ISRAMT'93)*, New Delhi, Agra, Dec. 1993.
6. **Member** *Photonics' 98*, An International Conference held in December, New Delhi, 1998.

NATIONAL

1. **Coordinator** Short course on *Electrical modeling and simulation of inter connects and packaging for digital and microwave modules* (at UDSC) December 15, 1996.
2. **Coordinator** Short course on *Active Integrated Antennas*, (at UDSC) December 16, 1996.
3. **Coordinator** Short course on *CAD of Microstrip Circuits and Antennas* (at UDSC) December 10-14, 1993.
4. **Coordinator** Short course on *Microwave Hyperthermia and Cancer*, (at UDSC) December 13-14, 1993.
5. **Member, Organising Committee** National Symposium on *Recent advances in microwaves and light waves (NSAML'95)*, University of Delhi South Campus, New Delhi, December 1995.
6. **Member** National symposium on *Advances in Microwaves (NSAM'93)* University of Delhi South Campus, New Delhi, March 1993.
7. **Member** National Symposium on *Recent advances in microwaves and light waves (NSAML'97)* University of Delhi South Campus, New Delhi, December 1997.
8. **Chairman Technical Committee** National Symposium on *Recent advances in microwaves and light waves (NSAML'2000)*, University of Delhi South Campus, New Delhi, March 2000.

9. **Coordinator** Intensive short course on *Modeling and Characterization of Microelectronics Devices*, March 27, 28, 2000.
10. **Vice-Chairman** National Symposium on *Recent advances in microwaves and light waves (NSAML'2003)*, University of Delhi South Campus, New Delhi, October 2003.
11. **Member** Short course on *Application of artificial neural networks to RF and microwave design*, December 13 – 14, 2004, New Delhi, India.
12. **Member** Short course on *Phased array antenna and adaptive beam forming arrays for radar and communication systems*, December 13 – 14, 2004, New Delhi, India.
13. **Coordinator** Short course on *Spice Models for Advanced VLSI Circuit Simulation (SMAVCS)*, 11-12 December, 2005.

9.

Personal publications **Separate sheet attached**

10.

**IEEE Award/Distinction**

- Best paper award on paper entitled “*A Comparative Analysis Using Modeling and Simulation to Study the Impact of Multilayered Gate Dielectric (MGD) Design on Device Performance of Surrounding Gate MOSFET*”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, XXIX General Assembly of the International Union of Radio Science, (Union Radio Scientifique Internationale – URSI), Illinois, USA, August 07-16, 2008.
- Name appeared for six consecutive years in the golden list published by IEEE Trans. Electron Devices (December 2002 – December 2007 in the history of the IEEE).
- Best paper award on paper entitled “*Design guidelines of vertical surrounding gate (VSG) MOSFETs for future ULSI circuit applications*” Abhinav Kranti, Rashmi, S. Haldar and R.S. Gupta, Topical Meeting (IEEE) on Silicon Monolithic Integrated circuits in RF systems, Ann Arbor, Michigan, U.S.A., September 2001.
- Name appeared in the golden list published by IEEE Trans. Electron Devices (December 1998 in the history of the IEEE).

11.

Research support to the investigator from various sources

- [1]. **UGC Sponsored** Threshold voltage dependence on channel length and extraction of Averages doping density and junction depth in small geometry MOSFETs for VLSI. *Completed*  
[Rs. 9.00 Lakhs]  
*Sanction Letter No.:*  
F.No. 9-2/88(SR-IV) Dt. 22.12.1989

[2].	<b>DRDO Sponsored</b>	Modeling simulation and characterization of Si/GaAs MOSFETs for high frequency applications. [Rs. 3.52 Lakhs] <i>Sanction Letter No.:</i> DTSR/70843/140/RD-82 Dt. 06.08.1991	<i>Completed</i>
[3].	<b>DRDO Sponsored</b>	A 2-Dimensional field dependent mobility model for ultra thin film fully depleted SOI (Silicon on Insulator) MOSFETs down to 0.1 $\mu\text{m}$ gate length at microwave frequencies. [Rs. 3.05 Lakhs] <i>Sanction Letter No.:</i> DTSR/70843/197/RD-82 Dt. 22.06.1994	<i>Completed</i>
[4].	<b>UGC Sponsored</b>	Analytical two-dimensional model for deep sub micrometer MOSFETs for VLSI/ULSI applications. [Rs. 5.10 Lakhs] <i>Sanction Letter No.:</i> F.21-2/93(SR.I) Dt. 17.01.1994	<i>Completed</i>
[5].	<b>DST Sponsored</b>	Two dimensional analytical modeling and simulation of Si and GaAs low noise MOSFET/MESFET devices for microwave frequency. [Rs. 7.48 Lakhs] <i>Sanction Letter No.:</i> III5(40)/95-ET Dt. 15.03.1996	<i>Completed</i>
[6].	<b>CSIR Sponsored</b>	Modeling and Simulation of (Al GaAs-GaAs) Modulation Doped Field Effect Transistors for Millimeter Microwave Integrated Circuits. [Rs. 3.6 Lakhs] <i>Sanction Letter No.:</i> 3(754)94-EMR-II Dt. 25/28.11.1994	<i>Completed</i>
[7].	<b>UGC Sponsored</b>	Analytical Model for Short Channel MOSFETs for VLSI/ULSI Applications [Rs. 3.47 Lakhs] <i>Sanction Letter No.:</i> 14-21/96(SR-I) Dt. 25.06.1996	<i>Completed</i>
[8].	<b>DRDO Sponsored</b>	Analytical modeling of hot carrier effects in submicrometer MOSFETs for VLSI/ULSI applications. [Rs. 5.74 Lakhs] <i>Sanction Letter No.:</i> DTSR/70685/Proj-6/R&T/4347/D(R&D), Dt. 19.09.1996	<i>Completed</i>
[9].	<b>AICTE Sponsored</b>	Modeling and Simulation of Solid State Microelectronic MOSFET/MESFET/HEMT Devices [Rs. 6.9 Lakhs] <i>Sanction Letter No.:</i> 8017/RDII/R&D/TAPTEC(622)/98-99, Dt. 27.03.1999	<i>Completed</i>
[10].	<b>DRDO Sponsored</b>	2-Dimensional Analytical/ Empirical Modelling and Characterisation of Small Geometry MOSFET/MESFET for Very High Frequency Applications. [Rs. 5.71 Lakhs] <i>Sanction Letter No.:</i> DTSR/70685/Proj-10/R&T/4725/D(R&D), Dt. 19.11.1998	<i>Completed</i>

[11].	<b>DRDO Sponsored</b>	Scattering and Temperature Dependent 2-D Analytical Modeling and Analysis of Submicron Surrounding Gate SOI MOSFET for its Microwave Frequency Applications. [Rs. 11.08 Lakhs] <i>Sanction Letter No.:</i> DTSR/70685/Proj-9/R&T/2189/D(R&D), Dt. 15.06.1999	<i>Completed</i>
[12].	<b>DRDO Sponsored</b>	Modulating Frequency and Scattering Dependent Optically Controlled Electrical Characteristics of Si/GaAs OPFET 77K-35K for its Potential Applications in Optical Communication System. [Rs. 11.18 Lakhs] <i>Sanction Letter No.:</i> DTSR/70685/Proj-8/R&T/6012/D(R&D), Dt. 13.10.1998	<i>Completed</i>
[13].	<b>DRDO Sponsored (Co-PI)</b>	Two-Dimensional Temperature and Bias Dependent Noise Analysis and Improved Equivalent Circuit Model of InP HEMTs for Microwave Characterization. [Rs.21.17 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0023012/M/01, Dt. 01.10.2001	<i>Completed</i>
[14].	<b>DRDO Sponsored</b>	Accurate Physics Based Analytical Modeling of 6H/SiC MOSFETs for High Power High Temperature and Microwave Frequency Applications. [Rs.20.47 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0103309/M/01/2127/D (R&D), Dt. 13.09.2001	<i>Completed</i>
[15].	<b>CSIR Sponsored</b>	Analytical 2-Dimensional Modeling Simulation and Characterization of AlGaIn/GaN HEMT/MESFET Devices for Microwave Frequency Applications [Rs. 5.88 Lakhs] <i>Sanction Letter No.:</i> 22(0330)/02/EMR-II, Dt. 11.01.2002	<i>Completed</i>
[16].	<b>DRDO Sponsored (ARMAMENT)</b>	Modeling, Simulation & Characterization of Silicon based Submicron Semiconductor Devices for Higher Design Reliability. [Rs. 24.75 Lakhs] <i>Sanction Letter No.:</i> DARM/20/20004/M/03, Dt. 09.01.2002	<i>Completed</i>
[17].	<b>DRDO Sponsored (Co-PI)</b>	Development & Characterization of Transparent Conducting Material for Optically Controlled Devices [Rs. 19.22 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0103325/M/01 Dt. 04.01.2002	<i>Completed</i>
[18].	<b>DST Sponsored</b>	Modeling Simulation and Characterization of Quantum Mechanical Effect in Nano Scale MOSFETs for ULSI Circuit Applications [Rs. 16.68 Lakhs] <i>Sanction Letter No.:</i> SR/S3/EE/013/2002-SERC-Engg., Dt. 11.12.2002	<i>Completed</i>

[19].	<b>DRDO Sponsored</b>	Design, Optimization and Simulation of Dual Material Gate (DMG)- Structure for Improved Hot-Electron Effect and Gate Transport Efficiency of Sub-100nm MOSFET for RF Applications [Rs. 22.62 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0203372/M/01, Dt. 10.12.2002	<i>Completed</i>
[20].	<b>DRDO Sponsored (Co-PI)</b>	Physics Based Modeling, Simulation and Electrical Characterization of a Novel Device Architecture: Silicon on Nothing (SON) MOSFET for Sub-100 nm Device Dimensions [Rs. 31.68 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0303417/M/01, Dt. 03.12.2003	<i>Completed</i>
[21].	<b>DRDO Sponsored</b>	Two-Dimensional Physics Based Modeling and Simulation of a Graded Channel (GC) Multiple SOI-MOSFET for Sub-100nm Device Dimensions for High Performance Analog Application [Rs. 13.37 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0303446M/01, Dt. 23.08.2004	<i>Completed</i>
[22].	<b>DRDO Sponsored</b>	Modeling Simulation & Characterization of Modified Double Gate Sub-100 nm MOSFET Structure for ULSI Circuit Applications [Rs. 11.73 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0403488/M/01, Dt 07.06.2005	<i>Completed</i>
[23].	<b>CSIR Sponsored</b>	Analytical Modeling and Simulation of Modulation Doped Field Effect Transistors (MODFET) [Rs. 14.03 Lakhs] <i>Sanction Letter No.:</i> 21(0710)/08/EMR-II Dt. 28.04.2008	<i>Completed</i>
[24].	<b>DRDO Sponsored (Co-PI)</b>	Modeling, Simulation & Characterization of Modified Different Gate Geometric High Electron Mobility Transistor for Tera Hertz Applications [Rs. 14.83 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/0503560/M/01/894, Dt. 15.06.2006	<i>Completed</i>
[25].	<b>DST Sponsored (Co-PI)</b>	Modeling, Simulation & Characterization of Modified Different Gate Geometric Double Gate High Electron Mobility Transistor for High Power and High Frequency Applications with Two Separate/Common Gate Control [Rs. 19.67 Lakhs] <i>Sanction Letter No.:</i> SR/S3/EECE/042/2007 Dt. 16.11.2007	<i>Completed</i>
[26].	<b>UGC (Co-PI)</b>	<i>Modeling and simulation of Nanoscale Dual Material Gate Insulated Shallow Extension Silicon on Nothing MOSFET for Low voltage low power applications</i> [Rs. 9.22 Lakhs] <i>Sanction Letter No.:</i> F. No. 36-258/2008(SR), May 2009 – May 2012	<i>Completed</i>
[27].	<b>AICTE Sponsored</b>	<i>Analytical Modeling simulation and characterization of Silicon Gate All Around Nanowire MOFET for Ultra Large Scale Integration circuit Applications</i> [Rs. 13.00 Lakh] <i>Sanction Letter No.:</i> 8023/RID/RPS/36/PVT(POLICY-II)/2011-2012	<i>Completed</i>



[28].	<b>DRDO Sponsored</b>  <b>(Co-PI)</b>	Analysis and Characterization of Silicon Gate All Around Nanowire MOSFET for ULSI Circuit Application [Rs. 30.62 Lakhs] <i>Sanction Letter No.:</i> ERIP/ER/1002196/M/011395, Dt. 26.12.2011	<i>Will be          completed          on 20-Feb          2016</i>
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## **12. Technical Visits Outside India**

1. Department of Electronics Engineering, University of Malaga, Spain, December 1999.
2. Department of Electronics and Electrical Engineering, University of Sheffield, U.K. (*May - July 1988*) - Visiting Scientist under ALIS Link UGC-British Council.
3. Progress in Electromagnetic Research Symposium (PIERS'95), Seattle, Washington U.S.A. - (*July 1995*).
4. Department of Electrical Engineering, Washington State University, Seattle Washington, U.S.A. - (*July 1995*).
5. Department of Electronics and Computer Engineering, Oregon State University, Oregon, U.S.A. - (*July 1995*).
6. Department of Electronics and Electrical Engineering, College of Engineering, University of Nevada Reno, U.S.A. - (*July 1995*).
7. Department of Electrical and Computer Engineering, University of Colorado, Boulder, U.S.A. - (*August 1995*).
8. Deptt. of Electronic and Electrical Engineering, University of Utah, U.S.A. - (*August 1995*).
9. Department of Electrical and Computer Engineering, College of Engineering, University of Toledo, U.S.A. - (*August 1995*).
10. University of Malaga, (*Spain 1999*).
11. Technical University of Ostrava, Czech Republic, (*August 2003*)
12. Asia-Pacific Microwave Conference (APMC-2003), Seoul, Korea, (*November 2003*)
13. Rensselaer Poly-technique Institute, New York, USA, (*August 2004*).
14. International Symposium on Microwave and Optical Technology (ISMOT-2005), Fukuoka Institute of Technology, Japan, (*August 2005*)
15. International Symposium on Microwave and Optical Technology (ISMOT-2007), University of Roma Tor Vergata, Italy, (*17 – 21 December 2007*)
16. Visiting Beijing, China attending IEEE-ED meeting, (*May 31- June 4, 2007*)
17. Visited University of North Texas, USA, (*May 2009*)
18. Visited Southeast Missouri State University – (*May 2009*)

## Invited Lectures Delivered at

1. Progress in Electromagnetic Research Symposium (PIERS'95), Washington State University, U.S.A. - (July 1995).
2. Lecture at University of Utah, U.S.A. - (July 1995).
3. Lecture and discussion in the research group college of Engineering, University of Toledo, U.S.A. - (August 1995)
4. Lectures at University of Nevada Reno, U.S.A. - (July 1995).
5. Special lectures on VLSI Design and technology at Dayal Bagh Educational Institute, Agra, - (October 1992).
6. Lecture on VLSI technology in refresher course for college teachers held at Draunacharya College, University of Rohtak - (January 1992).
7. Short term course for SC/ST students of B.Tech (of IITs) sponsored by DOE held at University of Delhi South Campus -
  - (i) June - July 1989
  - (ii) June - July 1990
8. Lecture on "Evolution of VLSI" in refresher course for college teachers under CPDHE program, University of Delhi, June 1998.
9. Lecture on "Semiconductor device development" for college teachers under CPDE program, University of Delhi, October 2001.
10. Lecture on "Evaluation of microelectronic devices" for college teachers organised by Jawahar Lal Nehru University, December 12-13, 2001.
11. Lecture on "Optimization of InAlAs/InGaAs heterostructure, InP based HEMT for its microwave frequency applications" Ostrava, Czech Republic, August 11-15, 2003.
12. Lecture on "Temperature dependent characterization of InAlAs/InGaAs/InP LMHEMT for microwave frequency application" Ostrava, Czech Republic, August 11-15, 2003.
13. Lecture on "Modeling of submicron field effect devices" Solid State Physics Laboratory, (Ministry of Defence) New Delhi, July 21, 2004.
14. Lecture on "Analytical model for non-self aligned buried p-layer SiC MESFET", 4 – 6, August, New York, 2004.
15. Lecture on "Two-dimensional analytical modeling and simulation of retrograde doped HMG MOSFET" 4 – 6, August, New York, 2004.
16. Lecture on "Two-Dimensional Analysis and Simulation for Gate Stack Silicon-on-Nothing MOSFET (GAS-SON) MOSFET" Fukuoka Institute of Technology Japan, August 22-25, 2005.
17. Lecture on "Modeling and Simulation of Poly-Crystalline Silicon Thin Film Transistor for Improved Gate Transport Efficiency" Fukuoka Institute of Technology Japan, August 22-25, 2005.

## 14. Book and Book Chapter

- [i]. **Recent Advances in Microwave Technology** R.S. Gupta (Ed.), *New Age International Publisher*, New Delhi, 1993.
- [ii]. **Analytical Modeling of Short Channel Devices** R.S. Gupta and Rachna Sood, Chapter in the book entitled *Recent Advances in Microwaves* (Ed. G.P. Srivastava), *Narosa Publishing House*, New Delhi, 1993.
- [iii]. **Proceedings Edited** *8<sup>th</sup> Asia-Pacific Microwave Conference (APMC '96)*, University of Delhi, Dec. 17-20, 1996, Hotel Ashok, New Delhi.
- [iv]. **Proceedings Edited** National Symposium on *Recent advances in microwaves and light waves (NSAML'2000)*, University of Delhi South Campus, New Delhi, March 2000.
- [v]. **Proceedings Edited** National Symposium on *Recent advances in microwaves and light waves (NSAML'2003)*, University of Delhi South Campus, New Delhi, October 2003.
- [vi]. **Proceedings Edited** *16<sup>th</sup> Asia-Pacific Microwave Conference (APMC '04)*, University of Delhi, (to be organized in Dec. 15-18, 2004, New Delhi.
- [vii]. **Proceedings Edited** *12th International Symposium on Microwave and Optical Technology (ISMOT-2009)*, University of Delhi, December 16–19, 2009, New Delhi, India.
- [viii]. **MOSFET Modeling** R.S. Gupta, Mridula Gupta and Manoj Saxena in *Encyclopedia of RF & Microwave Engineering*, John Wiley U.S.A. (Jan. 2005).

## 15. Academic (International)

### IEEE Activities

<i>Treasurer</i>	- IEEE-ED/MTT Chapter	1976 – 1978
<i>Secretary</i>	- IEEE-ED/MTT Chapter	1978 – 1980
<i>Vice Chairman</i>	- IEEE-ED/MTT Chapter	1980 – 1982
<i>Secretary</i>	- IEEE Delhi Section	1983 – 1984
<i>Member</i>	- IEEE/ED-MTT Chapter	1984 – 1990
<i>Member</i>	- IEEE/ED-MTT Chapter	1995 – 2000
<i>Chairman</i>	- IEEE/ED Chapter Delhi	2007 – 2011

## 16. Member Expert Committee

AICTE (*All India Council for Technical Education*) (U.P., Bihar, Rajasthan, Orissa, Karnataka, Maharashtra).

## 17. REVIEWER

### A. International Journal (Referred Journal)

1. IEEE Trans. Electron Devices
2. IEEE Electron Device Letter
3. IEEE Trans Microwave Theory and Techniques
4. Solid-State Electronics (Elsevier)
5. Journal of Microelectronics Engineering (Elsevier)
6. Journal of Vacuum (U.K.)
7. International Journal of Electronics (U.K.)
8. Journal of Microelectronics Reliability

#### B. Indian Journal

1. Indian Journal of Pure and Applied Physics (CSIR)
2. Indian Journal of Physics (Calcutta)
3. IETE Journal (The Institute of Electronics and Telecommunication Engg.)
4. Defence Science Journal (Ministry of Defence, Govt. of India)

**18.**  
**(A)**

#### Contributions to the corporate life of the Institution

1. **Coordinator** – Vocational Training Unit, University of Delhi – 1994 to 1999 (for SC/ST Students sponsored by DSFDC, Govt. of Delhi).
2. **Chairman** – Transport Committee, University of Delhi South Campus – 1993 to 2003.
3. **Coordinator** – B.Sc. (H) Electronic Course – University of Delhi South Campus – 1998 to till date.
4. **Coordinator** – B.Sc. B.A.Sc. Electronic/Instrumentation course, University of Delhi – 1994 to till date.
5. **Students Advisor** – Students Union – University of Delhi South Campus – 1989 – 1995, 1998 – 2008.
6. **Coordinator** – PG Exam South Campus – 1998 – 2003.
7. **Chairman Library Committee**, UDSC – 2002 – 2004.
8. **Chairman UFM Committee** (Examination Disciplinary Committee) – 1989 – 2004.
9. **Chairman** – Write-off Committee, UDSC – 2002 to continue.
10. **OSD**, Institute of Informatics and Communication, South Campus, September 2002 to January 2008.
11. **Member Managing Committee**, Institute of Informatics and Communication, South Campus, September 2002 to till date.
12. **Dean Student Welfare**, (University of Delhi South Campus) 1989-1997.
13. **Member governing bodies**
  1. Bhaskaracharya College of Applied Science – 2 Years
  2. College of Vocational Studies – 4 Years
  3. Dayal Singh College – 3 Years
  4. Ramlal Anand College – 2 Years

**(B) Corporate life in the Department****Coordinator B.Sc. (H) Electronics**

1988 – 1990

1992 – *Continue***Coordinator B.A. Sc. (Applied Science)**1992 – *Continue***Convener Purchase Committee**

1988 – 1990

1992 – 1997

2003 – *Continue***Convener Library Committee**

2000 – 2003

**Coordinator – M.Sc. (Electronics)****Member Board of Research Studies****TEACHING AND RESEARCH SUPERVISION****I. Major Projects Supervision**

- M.Sc. Project - 34
- M.Tech Project - 24
- M.Phil - 6

**PH.D. THESIS SUPERVISION**

S.No.	Name	Year	Title of the Thesis
1.	Subhasis Haldar	1994	<i>Analytical Modeling and Analysis of Depletion mode devices.</i>
2.	Alka Das	1994	<i>Electrical Characterization of Metal (P) a.Si : H (n) GaAs Heterostructures</i>
3.	Rachna Sood	1995	<i>An analytical two dimensional model for short channel ion implanted GaAs MESFET using perturbation method</i>
4.	Vaneeta Agarwal	1996	<i>A New two dimensional analytical model for short channel fully depleted thin film SOI MOSFETs</i>
5.	Maneesha	1996	<i>Analytical modeling and characterization of non uniformly doped short channel MOSFETs</i>
6.	Manoj K. Khanna	1997	<i>Anomalous Behavior &amp; Fringing Field Dependent Threshold Voltage Modeling of Small Geometry MOSFETs for VLSI Applications</i>
7.	Manju Bhatia	1997	<i>Analytical Subthreshold and Threshold Voltage Modelling for Small Geometry MOSFET</i>

8. S. Rajesh 1997 *Optimization of MESFETs With Pearson Approach Using Computer - Aided – Modelling: A Fuzzy Method for VLSI Design*
9. Ciby Thomas 1997 *Computer-Aided-Modelling and Analysis of Drain Engineered MOS Transistors for VLSI/ULSI Applications*
10. Sunita A Chhokra 1997 *An improved two dimensional analytical model with trial function approach for non self aligned GaAs MESFETs*
11. Rubeena Saleem 1999 *Modelling and Characterization of Small Geometry Metal Oxide Field Effect Transistor for Microwave Frequency Applications*
12. Sujata Sen 1999 *Al GaAs-GaAs Heterostructure modeling for microwave frequency application*
13. Manoj K Pandey 1999 *Two-Dimensional Analytical Modeling and Characterization of a Fully Depleted Double Gate SOI MOSFET Down to 0.1  $\mu\text{m}$  Gate Length*
14. Sonia Chopra 1999 *An Analytical Formulation for Computer-Aided-Modeling of Short Channel and Small Geometry Polycrystalline-Silicon Thin-Film Transistor*
15. Anju Agarwal 2000 *An Accurate Two-Dimensional Modeling of Pseudomorphic Modulation Doped Field Effect Transistor (AlGaAs/InGaAs) for Microwave and High-Speed Circuit Applications.*
16. Anil Kumar 2000 *An Analytical Model of Hot Carrier Immunized Submicron Fully Overlapped Lightly Doped Drain MOSFET for VLSI/ULSI Applications*
17. Ekta Kalra 2000 *Analytical Modeling and Characterization of Hot Carrier Resistant Small Geometry LDD MOSFETs for VLSI/ULSI Applications*
18. Anisha Goswami 2000 *Substrate Effect Dependent Scattering Parameters Extraction and Small-Signal MOSFET Circuit Analysis for Microwave Frequency Applications*
19. Srikanta Bose 2001 *Analytical Modeling of GaAs MESFET under Dark and Illuminated Conditions for MMIC/OEIC Applications*
20. Abhinav Kranti 2001 *Two-Dimensional Modeling and Characterization of Short Channel Vertical Cylindrical/Surrounding Gate SOI MOSFETs (CGT/SGT) for ULSI Circuit Applications*
21. Rashmi Gupta 2002 *Modeling and Characterization of Spontaneous and Piezoelectric Polarization Dependent Lattice Mismatched AlGaN/GaN High Electron Mobility Transistors (HEMTs) for Microwave and Millimeter Wave Applications*
22. Jyotika Jogi 2002 *Two-Dimensional Analytical Modeling of Ultra-High Speed InAlAs/InGaAs/InP Lattice Matched High Electron Mobility Transistors*
23. Ritesh Gupta 2003 *Modeling, Characterization and Optimization of InAlAs/InGaAs Heterojunction, InP based High Electron Mobility Transistor (HEMT) For Microwave and Millimeter Wave Frequency Applications*
24. Adarsh Singh 2004 *Analytical Modeling, Analysis and Characterization of GaN MESFET for Optoelectronic Applications*
25. Simrata Bindra 2004 *Theoretical Analysis and Study of Polysilicon Thin Film Transistors*
26. Nirupma Kapoor 2005 *Distributed Gate Resistance Dependent Modeling and Noise*

*Analysis of SOI MOSFETs*

27. Vandana Guru 2005 *Noise Modeling and Scattering Parameter Evaluation of AlGaAs/InGaAs/GaAs Pseudomorphic HEMT for Microwave Frequency Application*
28. Navneet Kaushik 2007 *Modeling and Simulation of 6H-SiC MOSFETs for High Power and High Temperature Applications*
29. Manoj Saxena 2007 *Physics Based Analytical Modeling and Simulation of Dual-Material Gate (DMG) MOSFET*
30. Amit Sehgal 2007 *Poly-crystalline silicon thin film transistors: modeling, simulation and characterization*
31. Tina Mangla 2007 *Modeling, simulation and characterization of nano scale MOSFETs with quantum mechanical effects and gate stack engineering for ULSI*
32. Sandeep Aggarwal 2008 *Correlation & enhancement of circuit parameters with device parameters of different metal-insulator geometric single/double/dual gate 4H-SiC MESFET with common and separate gate control*
33. Ravneet Kaur 2008 *Analytical analysis, characterization and simulation of sub-100 nm advance MOSFET designs for improved hot carrier reliability and RF/ Analog performance*
34. Poonam Kasturi 2008 *Modeling Simulation and Characterization of SON MOSFET*
35. Harsupreet Kaur 2008 *Modeling and simulation of channel and gate oxide engineered cylindrical/surrounding gate MOSFETs for ULSI applications*
36. Rishu Chaujar 2009 *Analytical modeling and simulation of gate electrode workfunction and dielectric engineered recessed channel MOSFET in Sub-100nm Regime*
37. Servin Rathi 2011 *Modeling, Simulation & Characterization of Modified Different Gate Geometric Double Gate High Electron Mobility Transistor for High Power and High Frequency Applications with Two Separate/Common Gate Control*
38. Rajni Gautam 2013 *Analytical Modelling, Simulation and Characterization of optically Controlled Gate Electrode Engineered Nanoscale MOSFET/MESFET Design*
39. Yogesh Pratap *In Progress* *Modeling and Characterization of Gate All Around Junctionless Transistor for Reliability Study and Digital Applications*

**OTHER PH.D. SCHOLARS SUPERVISED BUT NOT REGISTERED**

1. Kirti Goel 2007 *Two Dimensional Analytical Modeling and Simulation of Non-Uniformly Doped Dual Material Gate(DMG) and Triple Material Gate (TMG) MOSFET Structures*
2. Sneha Kabra 2008 *Modeling Simulation and Characterization of GaN MESFET*

3.	Parvesh	2009	<i>Polarization dependent analysis and characterization of AlGaIn/GaN HEMT</i>
4.	Sona P Kumar	2010	<i>Analysis , Modeling and Simulation of AlGaIn/GaN Modular Doped Field Effect Transistor</i>
5.	Rupendra Sharma	2010	<i>Two Dimensional Analytical Modeling and Simulation of Gate Misalignment Effect in Fully Depleted Double Gate MOSFET</i>
6.	Ruchika Aggarwal	2010	<i>Modeling, Characterization and Simulation of AlGaIn/GaN Metal Insulator Semiconductor Heterostructure Field Effect Transistor(MISHFET) for High Power Microwave Applications</i>
7.	Priyanka Malik	2011	<i>Analytical modeling and simulation of advanced MOSFET structures in sub-100nm regime</i>
8.	Pujarani Ghosh	2013	<i>Capacitive Modelling Simulation and Characterization of Surrounded/Cylindrical Gate MOSFET (SGT/CGT) for High Frequency Applications</i>
9.	Vandana Kumari	2013	<i>Modeling and Simulation of Nano Scale DMG ISE SON MOSFET for Low Voltage Low Power Applications</i>
10.	Monika Bhattacharya	2013	<i>Noise Modeling, Noise Performance Simulation and Study of Noise Characteristics of Double Gate InP based InAlAs/InGaAs HEMTs for high power and Tara Hertz Frequency Applications</i>
11.	Rakhi Narang	2013	<i>Analytical Modeling of Double Gate Tunneling Field Effect Transistor</i>
12.	Jay Hind Kumar Verma	<i>In Progress</i>	<i>Noise Analysis and Modeling of CGT/SGT MOSFETs</i>
13.	Manoj Kumar	<i>In Progress</i>	<i>Analytical Modeling Simulation and Characterization of Schottky Barrier Gate All Around MOSFET structures for low power applications.</i>
14.	Sonam Revari	<i>In Progress</i>	<i>Analytical Modeling and Simulation of Gate All Around MOSFET</i>
15.	Jaya Madan	<i>In Progress</i>	<i>Simulation and Analysis of Gate All Around Tunnel FET for High Performance Analog and RF Applications</i>
16.	Nitin Trivedi	<i>In Progress</i>	<i>Analytical Modeling and Simulation of Junction Accumulation Mode Cylindrical Surrounding Gate MOSFET</i>



## LIST OF PUBLICATIONS

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### *I. Papers in Reviewed Journal*

- [1]. "Variation of current gain in p-n-p junction transistors", R.S. Gupta, res. rep., R.E.R.L., B.H.U., Vol. 1, P. 25, 1968.
- [2]. "Stability of the darlington composite transistor", R.S. Gupta, International, Journal of Electronics (London), Vol. 26, P. 117, 1969.
- [3]. "Stability of the composite transistor", R.S. Gupta, International Journal of Electronics, Vol. 26, No. 26, P. 533, 1969.
- [4]. "Single stage amplified characteristics of the super-beta composite transistor", R.S. Gupta, International Journal Electronics, Vol. 27, P. 259, 1969.
- [5]. "Investigations of the variations of the voltage gain with stability factor and biasing resistance in Darlington composite transistor", R.S. Gupta, International Journal Electronics, Vol. 27, P.487, 1969.
- [6]. "Output resistance of the super-beta composite transistor", R.S. Gupta, Indian J. Pure & Appl. Physics, Vol.7, P.764, 1969.
- [7]. "Amplifier characteristics of super-alpha composite transistor", R.S. Gupta, International Journal Electronics, Vol.28, P.95, 1970.
- [8]. "Analysis of a composite transistor voltage amplifier circuit", R.S. Gupta Indian J. Pure & Appl. Physics, Vol.8, P.33, 1970.
- [9]. "Output resistance of super-alpha composite transistor", R.S. Gupta, Indian J. Pure & Appl. Physics, Vol.8, P.237, 1970.
- [10]. "Amplifier characteristics of darlington composite transistor", R.S. Gupta, Int. J. Electronics, Vol. 28, P. 237, 1970.
- [11]. "Stability factor of the darlington composite transistor", R.S. Gupta, International Journal Electronics, Vol.29, No.4, P.395, 1970.
- [12]. "Amplifier characteristics of complementary composite transistor", R.S. Gupta, Res. Rep., Radio & Electronics Research Lab., Inst. of Tech., B.H.U., Vol.2, P.1, 1970.
- [13]. "Investigations of the variation of the current gain in p-n-p junction transistor", R.S. Gupta, Journal of the Institution of Engineers, Vol. 52, P.103, 1971.
- [14]. "Effect of variation of load resistance on amplifier characteristics of complementary composite transistor", R.S. Gupta, Int. Journal Electronics Vol.30, No.1, P.55, 1971.
- [15]. "Effect of variation of generator resistance on output resistance of a complementary composite transistor", R.S. Gupta, International Journal Electronics, Vol. 21, No.5, P.595, 1972.
- [16]. "Measuring hybrid parameters of a composite transistor", R.S. Gupta, Inst. Telecom. Engrs. (India), Vol.18, No.5, P.209, 1972.
- [17]. "Gain and stability of a new composite transistor", R.S. Gupta, International Journal Electronics, Vol. 34, No.6, P.741, 1973.
- [18]. "Effect of variation of load resistance of amplifier characteristics of complementary composite transistor II", R.S. Gupta, Int. Journal Electronics, Vol. 34, No.6, P.859, 1973.
- [19]. "Measurement of barrier height and its controlling parameters of bulk barrier diodes", R.S. Gupta, G.S. Chilana, G.P. Srivastava, J. Appl. Physics, Vol.58, P.7898, 1985.

- [20]. "An analysis of majority carrier three layer bulk semiconductor unipolar diodes", R.S. Gupta, G.S. Chilana, G.P. Srivastava, *J. Appl. Physics*, Vol.59, P.1702, 1986.
- [21]. "Barrier height enhancement of triangular barrier diodes", R.S. Gupta, G.S. Chilana, G.P. Srivastava, *Journal of Applied Physics*, Vol. 18, P.4103, 1986.
- [22]. "A simplified approach to reduce the effective barrier height of triangular barrier structures", R.S. Gupta, G.S. Chilana & G.P. Srivastava, *Physical States Solidi*, Vol. 96, P..89, 1986.
- [23]. "Determination of barrier height and technological parameters of a triangular barrier diode", R.S. Gupta & G.S. Chilana, *Physical State Solidi*, Vol.100, P. 763, 1987.
- [24]. "Control of the barrier height of triangular barrier diodes by doping their intrinsic layers", R.S. Gupta & G.S. Chilana, *Journal Appl. Physics*, Vol.63, P.1207, 1988.
- [25]. "A method to Determine surface doping and substrate doping profile of n-channel MOSFETs", R.S. Gupta, C. Jagdish, G.S. Chilana & G.P. Srivastava, *Physical State Solidi*, Vol.110, P. 671-675, 1988.
- [26]. "A modified NORDE function for the measurement of series resistance and the voltage dependent barrier height of triangular barrier height", R.S. Gupta & G.S. Chilana, *J. Appl. Physics*, vol. P. 1989.
- [27]. "Determination of solar cell minority carrier life time by frequency dependent A.C. photovoltage measurement", R.S. Gupta, Alka Nagpal, G.S. Chilana, V.K. Jain & G.P. Srivastava, *J. Solar Cells* October P. 1990.
- [28]. "Electrical properties of boron doped hydro generated amorphous silicon and n-type GaAs hetero structure", Alka Nagpal, R S Gupta and G.P. Srivastava, *Journal of Applied Physics*, Vol. 70, P. 3730, 1991.
- [29]. "The temperature dependence of threshold voltage in double implanted MOSFET", S.K. Dwivedi, Subhasis Haldar and R.S. Gupta, *International Journal of Electronics*, Vol.73, No.1, P. 65-69, 1992.
- [30]. "Inverse narrow width effect and small geometry MOSFET threshold voltage model", Manju Bhatia & R.S. Gupta, *IEEE Trans. Elect. Devices*, vol. ED-40, No.3, P.681, 1993.
- [31]. "Substrate bias dependent threshold voltage model of short channel MOSFETs", Manoj K. Khanna, Subhasis Haldar, Maneesha & Rachna Sood, & R.S. Gupta, *Solid State Electronics*, Vol.36, No.4, P.661, 1993.
- [32]. "An analytical two dimensional perturbation method to model submicron GaAs MESFET", Nirupma Kukreja, & R.S. Gupta, *IEEE Trans. Microwave Theory and Technology*, Vol. MTT-41, March 1993.
- [33]. "Analytical modeling of short channel devices", Rachna Sood, & R.S. Gupta, *Recent Advances in Microwaves* (ED. G.P. Srivastava), Narosa Publication, P.332-352, 1993.
- [34]. "Threshold voltage shift in depletion mode IGFET", Subhasis Haldar, Manoj Kumar Khanna, Maneesha, Rachna Sood, Vaneeta Aggarwal and Manju, & R.S. Gupta, *Solid State Electronics*, Vol.37, No.2, P.377-379, 1994.
- [35]. "Analytical 2-D modeling for potential distribution and threshold voltage of short channel SOI (Silicon-on-Insulator) MOSFET's" Vaneeta Aggarwal, M. K. Khanna, R. Sood, S. Haldar & R.S. Gupta, *Solid State Electronics*, Vol.37, No.8, P.1537-1542, 1994.

- [36]. "A device model for an ion-implanted MESFET with half Pearson-IV half Gaussian distribution under post anneal conditions", Subhasis Haldar, Manoj K. Khanna, Maneesha, & R.S. Gupta, IEEE Trans Electron Devices, vol. 41 No.9, P.1674-1677, 1994.
- [37]. "Narrow Gate Effect on Depletion Model IGFET", Subhasis Haldar, Manoj K. Khanna & R.S. Gupta, Solid State Electronics, Vol.37, No.10, P.1717-1721, 1994.
- [38]. "Temperature Dependence Threshold Voltage Model of a Short Channel MOSFET", Manoj K. Khanna, Subhasis Haldar & R.S. Gupta, International Journal Electronics, Vol. 77, No. 3, P. 283-290, 1994.
- [39]. "A 2-D Analytic Field Dependent-Mobility Model for the I-V Characteristic of Thin-Film-Fully Depleted SOI MOSFETs, Vaneeta Agarwal & R.S. Gupta, Solid-State Electronics, vol. 38, No. 1, P. 261-264, 1995.
- [40]. "A New Two-Dimensional Short-Channel Model for the Drain Current-Voltage Characteristics of Fully Depleted SOI (Silicon-On-Insulator) MOSFET", International Journal of Electronics, V. Agarwal & R.S. Gupta, vol. 79, No. 3, p. 293-301, 1995.
- [41]. "Analytical Theory of Two Dimensional Charge Sheet Model of Short Channel MOSFET under Non Linear Charge Control", Maneesha, Subhasis Haldar, Manoj K. Khanna & R.S. Gupta, Solid State Electronics, vol. 38. P. 197-202, 1995.
- [42]. "An Empirical, Fringing Capacitance Threshold Voltage Models for Short Channel MOSFETs", Maneesha, Manoj K. Khanna, Subhasis Haldar & R.S. Gupta, Solid-State Electronic, vol. 39, P.1687-1691, 1996.
- [43]. "Optimisation of Si MESFET model with pearson distribution", S. Rajesh, Ciby Thomas & R.S. Gupta, International Journal of Electronics, vol. 81, P.275-283, 1996.
- [44]. "Sub-threshold current model with modified threshold voltage for submicrometer scale GaAs MESFET", Sunita Chhokra & R.S. Gupta, Journal Semiconductor Science & Technology, IOP, U.K., vol. 12, P. 331-337, 1997.
- [45]. "An analytical model for anomalous threshold voltage behavior of short channel MOSFET", Manoj K. Khanna, Subhasis Haldar, Ciby Thomas & R.S. Gupta, Solid State Electronics, vol. 41, No. 9, P. 1386-1388, 1997.
- [46]. "Influence of profile shape factors on intrinsic FET device capacitance under diffusion mechanism, S Rajesh, Ciby Thomas & R.S. Gupta, IEEE Trans. Electron Devices, vol. 45, No. 1, P. 334-336, 1998.
- [47]. "Frequency Optimisation of MESFET Model with Pearson Distribution (FMA)", S. Rajesh, Ciby Thomas & R.S. Gupta, International Journal of Electronics, vol. 84, No. 2, P. 105-116, 1998.
- [48]. "Effects of Pearson-IV-Distribution on Intrinsic Gate-Drain Capacitance for an Ion-Implanted Si MESFET", S. Rajesh & R.S. Gupta, Semiconductor Materials and Devices, Narosa Publishing House, New Delhi, India, P.235-240, 1998.
- [49]. "A Fuzzy Method to Optimise the Performance of Si d-MESFETs: Influence of Pearson Profile", S. Rajesh & R.S. Gupta, IETE Technical Review, vol. 15, Nos. 1 & 2, P. 59-64, January-April, 1998.
- [50]. "Optimisation of Submicrometer GaAs MESFET for Improved Performance", Sunita A Chhokra & R.S. Gupta, Int. Journal of Electronics, vol. 85, No. 2, P. 129-144, 1998.

- [51]. "Analytical Model for C-V and RF Characteristics and Transient Response of Submicrometer Non-Self-Aligned GaAs MESFET", Sunita A Chhokra & R.S. Gupta, *Solid-State Electronics, USA*, Vol. 42, No. 11, P. 1917-1924, 1998.
- [52]. "Cut Off Frequency and Transit Time Analysis of Lightly Doped Drain (LDD) MOSFETs", Ciby Thomas, S. Haldar, Manoj Khanna, S. Rajesh, K.K. Gupta & R.S. Gupta, *Microelectronics Reliability*, vol. 38, No. 12, P. 1955-1961, 1998.
- [53]. "Thermal Characterization of a Double-Gate SOI MOSFET" Manoj K. Pandey & Sujata Sen, R.S. Gupta, *Journal of Physics D: Applied Physics*, vol. 32, No. 3, P. 344-349, 1999.
- [54]. "A Fringing Field Dependent 2-D Model for Non-Uniformly Doped Short Channel MOSFETs", Rubeena Saleem, Ciby Thomas, S. Haldar, R.S. Gupta, *International Journal of Electronics*, vol. 86, No. 4, P. 381-390, April 1999.
- [55]. "A New Analytical Model to Determine the Drain Source Series Resistance of FOLD MOSFET", Anil Kumar, Ekta Kalra, Subhasis Haldar and R.S. Gupta, *Semiconductor Science and Technology*, vol. 14, No. 6, P. 489-495, 1999.
- [56]. "Transconductance Extraction for Pseudomorphic Modulation Doped Field Effect Transistor (AlGaAs/InGaAs) for Microwave and Millimeter Wave Applications", Anju Agarwal, Anisha Goswami, Sujata Sen and R.S. Gupta, *Microwave and Optical Technology Letters*, Vol. 22 No. 1 P. 41-48, July 1999.
- [57]. "Two-Dimensional C-V Model of AlGaAs/GaAs Modulation Doped Field Effect Transistor (MODFET) for High Frequency Applications", R.S. Gupta, Sujata Sen, Manoj K Pandey, *IEEE Trans Electron Devices*, Vol.ED-46, No. 9, P.1818-1823, 1999.
- [58]. "Optimization of Drain Engineered MOS Transistors for Microwave Frequency Applications", Ciby Thomas, Rubeena Saleem & R.S. Gupta, *IETE Technical Review*, Vol. 16, No. 2, P. 229-236, March April 1999.
- [59]. "Design Aspects of a Submicrometer Gate Length High Electron Mobility Transistor" Sujata Sen, Manoj K. Pandey & R.S. Gupta, *Special Issue of IETE Tech. Review*, Vol. 16. No. 2, P. 223-228, March-April 1999.
- [60]. "An Empirical Model for Temperature Dependent Threshold Voltage and Drain Current-Voltage Characteristics of Thin Film Short Channel SOI MOSFETs", Vaneeta Agrawal and R.S. Gupta, *Indian Journal of Pure & Applied Physics*, Vol. 37, No. 9, P. 683-688 1999.
- [61]. "Temperature Dependent Threshold Voltage Analysis of Surrounding/Cylindrical Gate Fully Depleted Thin Film SOI MOSFET in the Range 77K-520K", Abhinav Kranti, Subhasis Haldar and R.S. Gupta, *Microelectronic Engineering*, vol. 49, P. 273-286, 1999.
- [62]. "Capacitance-Voltage Characteristics and Cut-off Frequency of Pseudomorphic (AlGaAs/InGaAs) Modulation Doped Field Effect Transistor for Microwave and High Speed Circuit Applications" Anju Agrawal, Anisha Goswami, Sujata Sen and R.S. Gupta, *Microwave and Optical Technology Letters*, Vol. 23 No.5 P. 312-318 December 1999.
- [63]. "Current-Voltage characteristics and Small Signal Parameters of a AlGaAs/GaAs Modulation Doped Field Effect Transistor" Sujata Sen & Manoj K. Pandey and R.S.

- Gupta, International Journal of Electronics, Vol. 87 No.2, P. 137-152, 2000.
- [64]. "Temperature and Aluminium Composition Dependent Sheet Carrier Concentration at AlGaAs/GaAs Interface", Sujata Sen, Manoj K. Panday, Subhasis Haldar and R.S. Gupta, Journal of Physics D: Applied Physics, Vol.33, P. 18-23, 2000.
- [65]. "Substrate Effect Dependent Scattering Parameter Extraction of short Gate Length IGFET for Microwave Frequency Applications" Anisha Goswami, Anju Agrawal, Srikanta Bose, S. Haldar Mridula Gupta and R.S. Gupta, Microwave and Optical Technology Letters, Vol. 24 No.5 P. 341-348, 5 March 2000.
- [66]. "Current Voltage Characteristics and Field Distribution of Pseudomorphic (AlGaAs/InGaAs) Modulation Doped Field-effect Transistor for Microwave Circuit Application" Anju Agarwal, Anisha Goswami, Sujata Sen and R.S. Gupta, Microwave & Optical Technology Letters, vol. 24, No. 6, P. 407-412, 2000.
- [67]. "Subthreshold Conduction in Short Channel Polycrystalline-Silicon Thin Film Transistor", Sonia Chopra and R.S. Gupta, Semiconductor Science and Technology, Vol. 15 P. 197-202, 2000.
- [68]. "1/f Noise Model of Fully Overlapped Lightly Doped Drain MOSFET" Anil Kumar, Ekta Kalra, Subhasis Haldar and R.S. Gupta, IEEE Transaction on Electron Devices, Vol. 47, No. 7, P.1426-1430, July 2000.
- [69]. "Small Signal Analytical MOSFET Model for Microwave Frequency Applications", Anisha Goswami, Anju Agrawal, S. Haldar, Ciby Thomas, Mridula Gupta and R.S. Gupta, Microwave Optical Technology Letters, Vol. 25, P. 346-352, June 5, 2000.
- [70]. "Frequency Optimization of Pseudomorphic Modulation Doped Field Effect Transistor (AlGaAs/InGaAs) for Microwave and Millimeter Wave Applications" Anju Agrawal, Anisha Goswami, Sujata Sen and R.S. Gupta, Microwave and Optical Technology Letters, Vol.25, P. 377 – 383, June 20, 2000.
- [71]. "An analytical Model for Turn-on Characteristics of Short Channel Polycrystalline Silicon Thin Film Transistor for Circuit Simulation", Sonia Chopra and R.S. Gupta, Microelectronic Engineering, Vol. 54, P. 263-275, 2000.
- [72]. "Cut-Off Frequency and Optimum Noise Figure of GaAs OPFET", Srikanta Bose, Mridula Gupta and R.S. Gupta, Microwave and Optical Technology Letters Vol 26, No. 5, P. 279-282, September 2000.
- [73]. "Scaling Effects on Thermal and Gate Induced Noise of Small Geometry LDD MOSFETs", Ekta Kalra, Anil Kumar, Subhasis Haldar and R.S. Gupta, Academic Open Internet Journal Newsletter Volume 1 (10 May 2000) URL: <http://www.Acadjournal.com/2000/V1/part1/p1>.
- [74]. "Modelling of Short Geometry Polycrystalline-Silicon Thin-Film Transistor", Sonia Chopra and R.S. Gupta, IEEE Trans Electron Devices, Vol. 47, No. 12, P. 2444-2446, December 2000.
- [75]. "An Analytical Model for Current-Voltage Characteristics of Small Geometry Poly-Si Thin Film Transistor", Sonia Chopra and R.S. Gupta, Semiconductor Science and Technology, vol. 15, No. 11, P. 1065-1070, November 2000.
- [76]. "Extraction of Small – Signal Model Parameters of Silicon MOSFET for RF Applications." Anisha Goswami, Anju Agrawal, Mridula Gupta, R.S. Gupta, Microwave and Optical Technology Letters, Vol. 27, No. 5, P. 352-358, 2000.
- [77]. "Characterization of Small Geometry LDD MOSFETs with Non- Pinned Flatband

- Voltage”, Ekta Kalra, Anil Kumar, Subhasis Haldar, R.S. Gupta, Indian Journal of Pure and Applied Physics. Vol. 38, No.8, P. 552-557, 2000.
- [78]. “Analytical Model for DC Characteristics and Small Signal Parameters of AlGaIn/GaN Modulation Doped Field Effect Transistor for Microwave Circuit Applications” Rashmi, Anju Agarwal, S.Sen, S. Haldar and R.S. Gupta, Microwave and Optical Technology Letters, Vol 27, No. 6, P. 413-419, December 20, 2000.
- [79]. “Flicker Noise Modeling of Small Geometry LDD MOSFETs”, Ekta Kalra, Anil Kumar, Subhasis Haldar, R.S. Gupta, Microelectronics Journal, vol. 32, No. 2, P. 143-147, 2000.
- [80]. “Cut-Off Frequency and Transit Time analysis in Short Geometry Poly-Si Thin Film Transistors”, Sonia Chopra and R.S. Gupta, International Journal of Electronics, Vol. 88, No. 2, P. 127-143, 2001.
- [81]. “Low Frequency Generation-Recombination Noise in Fully Overlapped in Highly Doped Drain MOSFETs”, Anil Kumar, Ekta Kalra, Subhasis Haldar and R.S. Gupta Microelectronics Journal, Vol. 32, No. 1, P. 43-47, 2001.
- [82]. “An Analytical 2-Dimensional Model for Optically Controlled Thin Film Fully Depleted Surrounding/ Cylindrical Gate (SGT) MOSFET”, Abhinav Kranti, S. Haldar and R.S. Gupta, Microwave and Optical Technology Letters, Vol. 28, No. 2, 135-141, January 20, 2001.
- [83]. “A Semi-empirical Model for Small Geometry Effects in LDD MOSFETs”, Ekta Kalra, Anil Kumar, Subhasis Haldar and R.S. Gupta, Microelectronic Engineering, Vol. 56, No. 4, P. 261-272, 2001.
- [84]. “Id~Vd Characteristics of Optically Biased Short Channel GaAs MESFET”, Srikanta Bose, Mridula Gupta and R.S. Gupta, Microelectronics Journal, Vol. 32, P. 241-247, 2001.
- [85]. "Carrier Concentration Dependent Low Field Mobility Model for InAlAs/InGaAs/InP Lattice Matched HEMT for Microwave Applications", Jyotika Jogi, Mridula Gupta and R.S. Gupta, Microwave and Optical Technology Letters, Vol. 29, No.1, P. 66-70, April 5 2001.
- [86]. "2-D Analytical Model for Current Voltage Characteristics and Output Conductance of AlGaIn/GaN MODFET", Rashmi, S. Haldar and R.S. Gupta, Microwave and Optical Technology Letters, Vol. 29, No. 2, P. 117-123, April 20, 2001.
- [87]. "An Accurate 2-D Analytical Model for Short Channel Thin Film Fully Depleted Cylindrical/Surrounding Gate (CGT/SGT) MOSFET", Abhinav Kranti, S. Haldar and R.S. Gupta, Microelectronics Journal, Vol. 32, No. 4, P. 305-313, 2001.
- [88]. "Analytical Model for Threshold Voltage and I-V Characteristics of Fully Depleted Short Channel Cylindrical/Surrounding Gate MOSFET", Abhinav Kranti, S. Haldar & R.S. Gupta, Microelectronic Engineering, Vol. 56, No. 4, P. 241-259, 2001.
- [89]. “Optimisation of improved short-channel performance of surrounding/cylindrical gate MOSFETs” A. Kranti, Rashmi, S. Haldar and R.S. Gupta, Electronics Letters, Vol. 37, No. 8, P. 533-534, April 2001.
- [90]. “Unilateral power gain of optically biased GaAs MESFET”, Srikanta Bose, Adarsh and R.S. Gupta, Applied Microwave & Wireless, Vol. 13, No. 8, P. 68-77, 2001
- [91]. “Analysis of scattering parameters and the thermal noise of MOSFET for its microwave frequency applications” Anisha Goswami, Mridula Gupta and R.S. Gupta,

- Microwave and Optical Technology Letters, Vol. 31, No. 2, P. 97-105, 20 October 2001.
- [92]. “An analytical model for saturation drain current and substrate current of fully overlapped LDD MOSFET”, Anil Kumar, Ekta Kalra, Srikanta Bose, Adarsh Singh, Simrata Bindra, Subhasis Haldar and R S Gupta, Indian Journal of Pure and Applied Physics, Vol. 39, No. 11, P. 731-737, 2001.
- [93]. “A new extrinsic dc model for high speed lattice matched InAlAs/InGaAs/InP HEMT with a predicted 135 GHz cut-off frequency”, Jyotika Jogi, Mridula Gupta and R S Gupta, Microelectronics Journal, Vol. 32, No. 12, P. 925-930, 2001.
- [94]. “A complete analytical model of GaN MESFET for microwave frequency applications”, Adarsh, Srikanta Bose, Simrata, Anil Kumar, Mridula Gupta and R. S. Gupta, Microelectronics Journal, Vol. 32, No. 12, P. 983-990, 2001.
- [95]. “Admittance parameter and unilateral power gain evaluation of GaN MESFET for microwave circuit applications”, Adarsh, Srikanta Bose, Mridula Gupta and R S Gupta, Microwave and Optical Technology Letters, Vol. 31, No. 5, P. 387-393, December 5, 2001.
- [96]. “An accurate 2-D model for transconductance to current ratio and drain conductance of vertical surrounding gate (VSG) MOSEFTs for microwave circuit applications”, A. Kranti, Rashmi, S. Haldar and R.S. Gupta, Microwave and Optical Technology Letters, Vol. 31, No. 6, P. 415-421, December 20, 2001.
- [97]. “Optical Radiation and temperature dependent microwave performance of an optically biased GaAs metal-semiconductor field effect transistor” Srikanta Bose, Mridula Gupta, S. Haldar and R.S. Gupta, Optical Engineering, Vol. 41, No. 1, 190-199, Jan’ 2002.
- [98]. “Model for optically biased short channel GaAs MESFET”, Srikanta Bose, Adarsh Singh, Ritesh Gupta, Mridula Gupta, and R. S Gupta, Microwave and Optical Technology Letters, vol. 32, No. 2, P. 138-142, January 20, 2002.
- [99]. “An analytical parasitic resistance dependent Id-Vd model for planar doped InAlAs/InGaAs/InP HEMT using non-linear charge control analysis”, Ritesh Gupta, A Kranti, S Haldar, Mridula Gupta and R S Gupta, Microelectronic Engineering, vol. 60, No. 3-4, P. 323-337, 2002.
- [100]. “Parasitic element dependent scattering parameter evaluation of GaN MESFET”, A. Singh, S. Bose, Mridula Gupta and R.S. Gupta, Microwave and Optical Technology Letters, vol. 33, No. 1, P. 54-57, April 5, 2002.
- [101]. “An accurate two-dimensional CAD-oriented model of retrograde doped MOSFETs for improved short channel performance”, Abhinav Kranti, Rashmi, S Haldar and R S Gupta, Microelectronics Engineering, Vol. 60, P. 295-311, 2002
- [102]. “Charge sheet model of polysilicon thin film transistor” Simrata Bindra, S. Haldar and R.S. Gupta, Microelectronic Engineering, vol. 60, P. 381-393, 2002.
- [103]. “An analytical two-dimensional model for pulsed doped InP-based lattice-matched HEMTs for high frequency applications”, Ritesh Gupta, Mridula Gupta and R. S. Gupta, Indian Journal of Pure and Applied Physics, vol. 40, P. 342-349, May 2002.
- [104]. “An accurate charge control model for spontaneous and piezoelectric polarization dependent two-dimensional electron gas sheet charge density of lattice mismatched AlGaIn/GaN HEMTs”, Rashmi, A. Kranti, S. Haldar and R.S. Gupta, Solid State

- Electronics, vol. 46, P. 621-630, 2002.
- [105]. "An analytical two-dimensional model for drain-induced barrier lowering in sub-quarter-micrometer gate length InAlAs/InGaAs/InAlAs/InP LMHEMT" Joytika Jogi, Sujata Sen, Mridula Gupta and R.S. Gupta, *Microelectronics Journal*, vol. 33/8 P. 633-638, July, 2002.
- [106]. "Design and optimization of thin film fully depleted vertical surrounding gate MOSFETs for enhanced short channel immunity", Abhinav Kranti, Rashmi, S. Haldar and R.S. Gupta, *Solid-State Electronics*, vol. 46, No. 9, P. 1333-1338, 2002.
- [107]. "Impact of strain relaxation of AlGa<sub>N</sub> layer on 2-DEG sheet charge density and current voltage characteristics of Lattice mismatched Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN HEMTs", Rashmi, A. Kranti, S. Haldar and R.S. Gupta, *Microelectronics Journal*, Vol. 33, No. 3, P. 205-, 2002.
- [108]. "Model for dc and RF characteristics of optically biased GaN MESFET for electronic/optoelectronic microwave applications" Adarsh Singh, Anil Kumar, M. Gupta & R.S. Gupta, *Optical Engineering*, vol. 41, No. 11, P. 2915-2955, 2002.
- [109]. "Physics Based Analytical Modeling of Potential and Electrical Field Distribution in Dual Material Gate (DMG)-MOSFET for Improved Hot Electron Effect and Reduced DIBL", Manoj Saxena, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *IEEE Trans Electron Devices*, Vol. 49, No. 11, P. 1928-1938, 2002.
- [110]. "Modeling of kink effect in polysilicon thin film transistor using charge sheet approach", Simrata Bindra, Subhasis Haldar and R.S. Gupta, *Solid-State Electronics*, Vol. 47/4 P. 645-651, 2003.
- [111]. "A New Depletion dependent Analytical Model for Sheet Carrier Density of InAlAs/InGaAs heterostructure, InP based HEMT" Ritesh Gupta, Mridula Gupta and R. S. Gupta, *Solid State Electronics* vol. 47, No. 1, P. 33-38, 2003.
- [112]. "Design and Optimization of Vertical Surrounding Gate (VSG) MOSFETs for Enhanced Transconductance-to-Current Ratio ( $gm/Ids$ )", Abhinav Kranti, Rashmi and R.S. Gupta, *Solid-State Electronics*, vol. 47, P. 155-159, 2003.
- [113]. "High frequency noise in fully overlapped lightly doped drain MOSFETs", Anil Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Microelectronics Engineering*, Vol. 65/3, P. 249-257, 2003.
- [114]. "Comprehensive Analysis of Small Signal Parameters of Fully Strained and Partially Relaxed High Al-content Lattice Mismatched Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN HEMTs", Rashmi, Abhinav Kranti, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *IEEE Trans MTT*, Vol. 51, No. 2, P. 607-617, 2003.
- [115]. "Extraction Technique for Characterization of Electric Field Distribution and Drain Current in VDMOS Power Transistor", Navneet Kaushik, Abhinav Kranti, Mridula Gupta and R.S. Gupta, *Microelectronics Journal*, vol. 34, No. 1, P. 77-83, 2003.
- [116]. "Physics Based Modeling and Simulation of Dual Material Gate Stack (DUMGAS) MOSFET", Manoj Saxena, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Electronics Letters*, Vol. 39, No. 1, (9th Jan.) P. 155-157, 2003.
- [117]. "Modeling Characterization and Optimization of Tri – Step doped InAlAs/InGaAs Heterostructure, InP based HEMT for Microwave Frequency Applications", Ritesh Gupta, Mridula Gupta and R. S. Gupta, *Indian Journal of Pure and Applied Physics*, Vol. 41, P. 223-231, March 2003.



- [118]. “A Distributed Network Model of SOI MOSFET for Microwave Frequency Applications” Nirupma Kapoor, Subhasis Haldar, Mridula Gupta and R.S Gupta, *Microwave and Optical Technology Letters*, Vol 37, No. 1, P. 26-31, April 5, 2003.
- [119]. “Analytical Model of 6H-SiC MOSFET”, Anil Kumar, Navneet Kaushik, Subhasis Haldar, Mridula Gupta and R. S. Gupta, *Microelectronic Engineering*, vol. 65, No. 4, P. 416– 427, 2003.
- [120]. “An Improved Intrinsic Small-Signal Equivalent Circuit Model of Delta-Doped AlGaAs/InGa/As/GaAs HEMT for Microwave Frequency Applications” Vandana Guru, Jyotika Jogi, Mridula Gupta, H. P. Vyas and R. S. Gupta, *Microwave and Optical Technology Letters*, vol. 37, No. 5, P. 376-379, (June) 2003.
- [121]. “Model for illumination dependent trap occupancy in optically biased GaN MESFET for improved electrical characteristics” Adarsh, Mridula Gupta and R.S. Gupta, *Optical Engineering*, vol. 42, No. 9, P. 2563-2567, (September) 2003.
- [122]. “Parasitic Resistance and Polarization Dependent Polynomial Based Non-Linear Analytical Charge-Control Model for AlGaIn/GaN MODFET for Microwave Frequency Applications” Manju Korwal, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Microwave and Optical Technology Letters*, vol. 38, No. 5 P. 371-378, (Sept.) 2003.
- [123]. “Modeling and simulation of asymmetric gate stack (ASYMGAS)-MOSFET” Manoj Saxena, Subhasis Haldar, Mridula Gupta, R.S. Gupta, *Solid-State Electronics*, vol. 47, P. 2131-2134, 2003.
- [124]. “Self Heating Dependent Thermal Noise Model using Distributed Gate Structure for RF Applications” Nirupama Kapoor, Subhasis Haldar, Mridula Gupta and R S Gupta, *Microwave and Optical Technology Letters*, vol. 40, No. 1, P. 87 – 92, (Jan 5) 2004.
- [125]. “Modeling power VDMOSFET transistors: Device physics and equivalent circuit model with parameter extraction”, Rakesh Vaid, Naresh Padha, Anil Kumar, R.S. Gupta and Chetan D. Parikh, *Indian Journal of Pure & Applied Physics*, Vol. 42, P. 775-782, October 2004.
- [126]. “A new simplified analytical short-channel threshold voltage model for InAlAs/InGaAs heterostructure InP based pulsed doped HEMT” Ritesh Gupta, Mridula Gupta and R.S. Gupta, *Solid-State Electronics*, vol. 48, No. 3, P. 437-443, March 2004.
- [127]. “Gate capacitance characteristics of a poly-Si thin film transistor” Simrata Bindra, Subhasis Haldar and R.S. Gupta, *Solid-State Electronics*, vol. 48, No. 5, P. 675-681, May 2004.
- [128]. “Analytical noise model of a high electron mobility transistor for microwave frequency application” Vandana Guru, H.P. Vyas, Mridula Gupta and R.S. Gupta, *Microwave and Optical Technology Letters*, vol. 40, No. 5, P. 410 – 417, 2004.
- [129]. “Numerical modeling and simulation of non- uniformly doped channel 6H-silicon carbide MOSFET” Navneet Kaushik, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Semiconductor Science and Technology*, vol. 19, P. 373-379, 2004.
- [130]. “Modelling of threshold voltage adjustment in fully depleted double gate (DG) SOI MOSFETs in volume inversion to quantify requirements of gate materials” Abhinav Kranti, Rashmi, S. Haldar and R.S. Gupta, *Indian Journal of Pure & Applied Physics*, vol. 42, P. 211 – 220, March 2004.

- [131]. “Design considerations for novel device architecture: Hetro -Material Double-Gate (HEM-DG) MOSFET with sub –100 nm gate length” Manoj Saxena, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Solid-State Electronics*, vol. 48, P. 1169 – 1174, 2004.
- [132]. “Accurate Charge Control Model Based Analysis of Noise Properties for AlGaAs/GaAs HEMT and AlGaAs/InGaAs PHEMT at Microwave Frequencies” Vandana Guru, Mridula Gupta, H. P. Vyas and R. S. Gupta, *Microwave and Optical Technology Letters*, vol. 42, No. 6, Pp. 489- 494, 2004.
- [133]. “Optimization of Gate Stack MOSFETs with Quantization Effects” Tina Mangala, Amit Sehgal, Manoj Saxena, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Journal of Semiconductor Technology and Science*, vol. 4, No. 3, Pp. 228 – 239, (September) 2004.
- [134]. “Optimization of InAlAs/InGaAs HEMT Performance for Microwave Frequency Applications and Reliability” Ritesh Gupta, Sandeep Kumar Aggarwal, Mridula Gupta and R.S. Gupta, *Journal of Semiconductor Technology and Science*, vol. 4, No. 3, Pp. 240 – 249, (September) 2004.
- [135]. “Analytical model for non-self aligned buried p-layer SiC MESFET”, Sandeep K. Aggarwal, Ritesh Gupta, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *International Journal of High Speed Electronics and Systems*, Vol. 14, No. 3, Pp. 897 – 905, 2004
- [136]. “Two-dimensional analytical modeling and simulation of retrograde doped HMG MOSFET” R.S. Gupta, K. Goel, M. Saxena and M. Gupta, *International Journal of High Speed Electronics and Systems*, Vol. 14, No. 3, Pp. 676 – 683, 2004
- [137]. “Analytical non-linear charge Control Model for InAlAs/InGaAs/InAlAs Double Heterostructure High Electron Mobility Transistor DH-HEMT”, Ritesh Gupta, Sandeep Kr Aggarwal, Mridula Gupta and R. S. Gupta, *Solid State Electronics*, Vol. 49, no.2, pp. 167-174, 2005.
- [138]. “Two-Dimensional Analytical Threshold Voltage Model for Dual Material Gate (DMG) Epi-MOSFET” Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, *IEEE Electron Devices*, vol. 52. No. 1, Pp.23-29 (January) 2005.
- [139]. “Temperature dependence on electrical characteristics of short geometry polycrystalline silicon thin film transistor” Amit Sehgal, Tina Mangla, Mridula Gupta and R.S. Gupta, *Solid-State Electronics*, Vol. 49, No. 3, Pp. 301-309, 2005.
- [140]. “A physics based analytical model for buried p-layer non-self aligned SiC MESFET for the saturation region”, Sandeep Kr. Aggarwal, Ritesh Gupta, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Solid State ductor*, Vol. 49, Pp. 1206-1212, 2005.
- [141]. “Channel Thermal Noise of SOI MOSFET in High Frequency Region”, Nirupama Kapoor, Subhasis Haldar, Mridula Gupta and R. S. Gupta, *Semiconductor Science and Technology*, vol. 20, Pp. 216-220, 2005.
- [142]. “Sub Threshold Analysis and Drain Current Modeling of Poly-Silicon Thin Film Transistor using Green’s Function Approach”, Amit Sehgal, Tina Mangla, Sonia Chopra, Mridula Gupta and R.S. Gupta, *IEEE Trans. Microwave Theory and Techniques*, vol. 53, No. 9, Pp. 2682-2687, 2005.
- [143]. “Analytical Model for High Temperature Performance of Non-self aligned SiC MESFET”, Sandeep Kr. Aggarwal, Ritesh Gupta, Subhasis Haldar, Mridula Gupta

- and R.S. Gupta, Indian Journal of Pure and Applied Physics, vol. 43, Pp. 697-704, (September) 2005.
- [144]. "Physics-based algorithm implementation for characterization of gate-dielectric engineered MOSFETs including Quantization effects" Tina Mangla, Amit Sehgal, Manoj, Saxena, Subhasis Halder, Mridula Gupta and R.S. Gupta, Journal of Semiconductor Technology and Science, Vol. 5, No. 3, Pp. 159-167, September 2005.
- [145]. "Evaluation of Scattering Parameters, Gain, and Feedback Capacitance Dependent Noise Performance of a pseudomorphic High Electron Mobility Transistor" Vandana Guru, H. P. Vyas, Mridula Gupta, R. S. Gupta, Microwave and Optical Technology Letters, Vol. 47, No. 1, Pp. 51-57, October 2005.
- [146]. "Interface Traps Distribution and Temperature Dependent 6H-SiC MOSFET Analysis", Navneet Kaushik, Subhasis Halder, Mridula Gupta and R. S. Gupta, Semiconductor Science and Technology, Vol. 21, Pp. 6-12, 2006.
- [147]. "Enhancement in performance of poly-crystalline thin film transistors with gate dielectric and work function" Amit Sehgal, Tina Mangla, Sonia Chopra, Mridula Gupta and R.S. Gupta, Thin Solid Films, Vol. 504, No. 1-2, Pp. 55-58, 2006.
- [148]. "Physics based threshold voltage extraction and simulation for poly-crystalline thin film transistors using double gate structure" Amit Sehgal, Tina Mangla, Mridula Gupta and R.S. Gupta, Semiconductor Science and Technology, vol. 21, Pp. 370-377, 2006.
- [149]. "Modeling and simulation of a nanoscale three region Tri material Gate stack (TRIMAGAS) MOSFET for improved carrier transport efficiency and reduced hot electron effects" Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, IEEE Trans. Electron Devices, Vol. 53, No. 7, Pp. 1623-1633, 2006.
- [150]. "An Analytical Model for Discretized Doped InAlAs/InGaAs heterojunction HEMT for Higher Cut-Off Frequency and Reliability" Ritesh Gupta, Sandeep Kr. Aggarwal, Mridula Gupta and R.S. Gupta, Microelectronics Journal, Vol. 37, No. 9, Pp. 919-929, 2006.
- [151]. "An Analytical Model for GaN MESFETs Using New Velocity-Field Dependence" Sneha Kabra, Harsupreet Kaur, Subhasis Halder, Mridula Gupta and R.S. Gupta, Physica Status Solidi, Vol. 3, No. 6, Pp. 2350-2355, 2006.
- [152]. "A Semi Empirical Approach for Submicron GaN MESFET Using an Accurate Velocity Field Relationship for High Power Applications" Sneha Kabra, Harsupreet Kaur, Ritesh Gupta, Subhasis Halder, Mridula Gupta and R. S. Gupta, Microelectronics Journal, Vol. 37, No. 1, Pp. 620-626, 2006.
- [153]. "Enhancement o in performance of sub-100nm MOSFETs with gate stack architecture" Tina Mangla, Amit Sehgal, Mridula Gupta and R.S. Gupta, International Journal of wave and Optical Technology (IJMOT), Vol. 1, No. 1, Pp. 106-113, (Online Journal), June 2006.
- [154]. "An analysis for AlGaIn/GaN modulation doped field effect transistor using accurate velocity-field dependence for high power microwave frequency applications" Sona P. Kumar, Anju Aggarwal, Sneha Kabra, Mridula Gupta and R.S. Gupta, Microelectronics Journal, Vol. 37, Pp. 1339-1346, 2006.
- [155]. "Modeling challenges in sub-100nm gate stack MOSFETs" Tina Mangla, Amit

- Sehgal, Mridula Gupta and R.S. Gupta, Semiconductor Science and Technology, Vol. 21, Pp. 1609-1619, 2006.
- [156]. "Analytical Model for Metal insulator Semiconductor High Electron Mobility Transistor (MISHEMT) for its high frequency and high power applications" Ritesh Gupta, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Journal of Semiconductor Technology and Science, Vol. 6, No. 3, Pp. 189-198, 2006.
- [157]. "Modeling Aspects of Sub-100nm MOSFETs for ULSI Device Applications" Tina Mangla, Amit Sehgal, Mridula Gupta and R.S. Gupta, IEEE Trnas. Electron Devices, Vol. 54, No. 1, Pp. 68-77, 2007.
- [158]. "Performance Investigation of 50nm Insulated Shallow Extension Gate Stack (ISEGaS) MOSFET for Mixed Mode Applications", Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, IEEE Transactions on Electron Devices, Vol. 54, No.2, pp. 365-368, February 2007.
- [159]. "Polarization dependent analysis of AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT for high power applications" Parvesh, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Solid State Electronics, Vol. 51, Pp. 108-113, 2007.
- [160]. "Impact of graded channel (GC) design in fully depleted cylindrical/surrounding gate MOSFET (FD CGT/SGT) for improved short channel immunity and hot carrier reliability" Harsupreet Kaur, Sneha Kabra, Simrata Bindra, Subhasis Haldar, and R.S. Gupta, Solid-State Electronics, Vol. 51, 398-404, (March) 2007.
- [161]. "Unified model for physics based modeling of a new device architecture: Triple Material Gate Oxide Stack Epitaxial Channel Profile (TRIMGAS Epi) MOSFET" Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, Semiconductor Science and Technology, Vol. 22, No. 4, Pp.435-446 , 2007.
- [162]. "Short channel analytical model for high electron mobility transistor to obtain higher cut-off frequency maintaining the reliability of the device", Ritesh Gupta, Sandeep Kr. Aggarwal, Mridula Gupta and R.S. Gupta, Journal of Semiconductor Technology and Science, Vol. 7, No. 2, P. 120-131, June 2007.
- [163]. "Hot carrier reliability and analog performance investigation of DMG-ISEGaS MOSFET", Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta, IEEE Transactions on Electron Devices, Vol. 54, No. 9, pp. 2556-2561, September 2007.
- [164]. "Unified Subthreshold Model for Channel Engineered Sub-100nm Advanced MOSFET Structures", Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, IEEE Transactions on Electron Devices Vol. 54, No. 9, pp. 2475-2486, September 2007.
- [165]. "Two-Dimensional Analytical Model to Characterize Novel MOSFET Architecture: Insulated Shallow Extension (ISE) MOSFET", Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta Semiconductor Science Technology, Vol.22, pp. 952-962, 2007.
- [166]. "Lateral channel engineered- hetero material insulated shallow extension gate stack (HMISEGAS) MOSFET structure: high performance RF solution for MOS technology", Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta Semiconductor Science Technology, Vol. 22, No.10, pp. 1097-1103, 2007.
- [167]. "A Semi-Empirical Model for Admittance and Scattering Parameters of Ga<sub>N</sub> MESFET for microwave circuit applications" Sneha Kabra, Harsupreet Kaur,

- Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Microwave and Optical Technology Letters*, Vol. 49, No. 10, Pp.2446-2450, 2007.
- [168]. "Threshold Voltage Model For Small Geometry AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs Based on Analytical Solution of 3-D Poisson's Equation" Sona P. Kumar, Anju Aggarwal, Rishu Chaujar, Sneha Kabra, Mridula Gupta and R.S. Gupta, *Microelectronics Journal*, Vol. 38, Pp. 1013-1020, 2007.
- [169]. "A compact C–V model for 120 nm AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT with modified field dependent mobility for high frequency applications", Parvesh Gangwani, Sujata Pandey, Subhasis Haldar, Mridula Gupta, R.S. Gupta, *Microelectronics Journal*, Volume 38, Issues 8–9, August–September 2007, Pages 848-854.
- [170]. "Poly-crystalline silicon thin film transistor: a two-dimensional threshold voltage analysis using green's function approach", Amit Sehgal, Tina Mangla, Mridula Gupta and R.S. Gupta, *Journal of Semiconductor Technology and Science*, Vol. 7, No. 4, Pp. 287 – 298, 2007.
- [171]. "Temperature dependent analytical model of sub-micron Ga<sub>N</sub> MESFETs for microwave frequency applications" Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S. Gupta, *Solid State Electronics*, Vol. 52, Pp. 25-30, 2008.
- [172]. "Multi-material gate poly-crystalline thin film transistors: Modeling and simulation for an improved gate transport efficiency", version 3 Amit Sehgal, Tina Mangla, Mridula Gupta, R. S. Gupta, *Thin Solid Films*, Vol. No. 516, Pp. 2162-2170, 2008.
- [173]. "Analytical Performance Evaluation of AlGa<sub>N</sub>/Ga<sub>N</sub> Metal Insulator Semiconductor Heterostructure Field Effect Transistor (MISHFET) and its Comparison with Conventional HFETs for High Power Microwave Applications" Ruchika Aggarwal, Anju Agrawal, Mridula Gupta and R.S. Gupta, *Microwave and Optical Technology Letters*, Vol. 50, No. 2, P.331 – 338, (February) 2008.
- [174]. "Laterally amalgamated Dual Material Gate Concave (L-DUMGAC) MOSFET for ULSI", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *Microelectronic Engineering*, Vol. 85, Pp. 566 – 576, March 2008.
- [175]. "Dual Material Double Layer Gate Stack SON MOSFET: A Novel Architecture for enhanced analog performance – Part I Impact of Gate Metal Workfunction Engineering", Poonam Kasturi, Manoj Saxena, Mridula Gupta and R.S. Gupta, *IEEE Transactions on Electron Devices*, Vol. 55, No. 1, Pp. 372-381, 2008.
- [176]. "Dual Material Double Layer Gate Stack SON MOSFET: A Novel Architecture for enhanced analog performance – Part II Impact of Gate Dielectric Material Engineering", Poonam Kasturi, Manoj Saxena, Mridula Gupta and R.S. Gupta, *IEEE Transactions on Electron Devices*, Vol. 55, No. 1, Pp. 382-387, 2008.
- [177]. "Two-dimensional analytical sub-threshold model of multi-layered gate dielectric recessed channel (MLaG-RC) nanoscale MOSFET", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *Semiconductor Science and Technology*, Vol. 23, No. 4, (10pp), April 2008.
- [178]. "Analytical modeling and simulation of subthreshold behavior in nanoscale dual material gate AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT" Sona P. Kumar, Anju Agrawal, Rishu Chaujar, Mridula Gupta and R.S. Gupta, *Superlattices and Microstructures*, Vol. 44, No. Pp. 37-53, July 2008.

- [179]. "Graded Channel Architecture: the Solution for Misaligned DG FD SOI n-MOSFETs", Rupendra Kumar Sharma, Ritesh Gupta, Mridula Gupta and R. S. Gupta, *Semiconductor Science and Technology*, Vol. 23, No. 7, Pp., 075041, 2008.
- [180]. "Intermodulation Distortion and Linearity Performance Assessment of 50-nm gate length LDUMGAC MOSFET for RFIC Design" Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *Superlattices and Microstructures*, Vol. 44, Pp.143-152, 2008.
- [181]. "TCAD Assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its Multi-Layered Gate Architecture: Part-I: Hot Carrier Reliability Evaluation" Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *IEEE Transactions on Electron Devices*, Vol. 55, No. 10, Pp. 2602-2613, 2008.
- [182]. "Gate Dielectric Engineering of Quarter Sub Micron AlGaIn/GaN MISHFET: A New Device Architecture for Improved Transconductance and High Cut-off Frequency", Ruchika Aggarwal, Anju Agrawal, Mridula Gupta and R.S. Gupta, *Solid State Electronics*, Vol. 52, Pp. 1610-1614, 2008.
- [183]. "On-State and RF Performance Investigation of Sub-50nm L-DUMGAC MOSFET Design for High-Speed Logic and Switching Applications" Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *Semiconductor Science and Technology*, Vol. 23, 095009 (8pp), 2008.
- [184]. "Modeling and Analysis of Fully Strained and Partially Relaxed Lattice Mismatched AlGaIn/GaN HEMT for High Temperature Applications", Parvesh Gangwani, Ravneet Kaur, Sujata Pandey, Subhasis Halder, Mridula Gupta and R.S. Gupta, *Superlattices and Microstructures*, Vol. 44, No. 6, Pp. 781-793, Dec. 2008.
- [185]. "Two Dimensional Simulation and Analytical Modeling of a Novel ISE MOSFET with Gate Stack Configuration", Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *Microelectronic Engineering*, Vol. 86, Pp. 2005-2014, 2009.
- [186]. "T-gate geometric (solution for submicrometer gate length) HEMT: Physical analysis, modeling and implementation as parasitic elements and its usage as dual gate for variable gain amplifiers" Ritesh Gupta, Servin Rathi, Ravneet Kaur, Mridula Gupta, R.S. Gupta, *Superlattices and Microstructures*, Vol. 45, No. 3, Pp. 105-116, 2009.
- [187]. "Investigation of Multi-Layered-Gate Electrode Workfunction Engineered Recessed Channel (MLGEWE-RC) Sub-50nm MOSFET: A Novel Design", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, Vol. 22, No. 3, Pp. 259-278, May/June 2009.
- [188]. "Two-dimensional threshold voltage model and design considerations for gate electrode workfunction engineered recessed channel (GEWE-RC) nanoscale MOSFET: part I", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, *Semiconductor Science Technology*, Vol. 24, No 6, 065005 (10pp), (June 2009)
- [189]. "Dynamic Performance of Graded Channel DG FD SOI n-MOSFETs for Minimizing the Gate Misalignment Effect", Rupendra Kumar Sharma, Mridula Gupta and R.S. Gupta, *Microelectronics Reliability*, Vol. 49, No. 6, pp. 592-599, June 2009
- [190]. "Dual-material double-gate SOI n-MOSFET: Gate misalignment analysis", Rupendra

- Kumar Sharma, Ritesh Gupta, Mridula Gupta and R.S. Gupta, IEEE Transactions on Electron Devices, Vol. 56, No. 6, 1284–1291, 2009.
- [191]. “TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multi-layered gate architecture: Part II: Analog and large signal performance evaluation”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, Superlattices and Microstructures, Vol. 46, No. 4, Pp. 645-655, October 2009.
- [192]. “Modeling of hetero-interface potential and threshold voltage for tied and separate nanoscale InAlAs-InGaAs symmetric double-gate HEMT”, Servin Rathi, Jyotika Jogi, Mridula Gupta, R.S. Gupta, Microelectronics Reliability, Vol. 49, pp. 1508-1514, 2009.
- [193]. “Design considerations and impact of technological parametric variations on RF/microwave performance of GEWE-RC MOSFET” Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, Microwave and Optical Technology Letters, Vol. 53, No. 3, P.652-657, 2010.
- [194]. “TCAD Performance Investigation of a Novel MOSFET Architecture of Dual Material Gate Insulated Shallow Extension Silicon On Nothing (DMG ISE SON) MOSFET for ULSI era” Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, Microwave and Optical Technology Letters, Vol. 53, No. 3, P.746-750, 2010.
- [195]. “Gate Material Engineered-Trapezoidal Recessed Channel MOSFET (GME-TRC) for Ultra Large Scale Integration (ULSI)” Priyanka Malik, Sona P. Kumar, Rishu Chaujar, Mridula Gupta & R.S. Gupta, Microwave and Optical Technology Letters, Vol. 53, No. 3, P.694-698, 2010.
- [196]. “Metal Insulator Gate Geometric HEMT: Novel Attributes and Design Consideration for High Speed Analog Applications”, Ritesh Gupta, Ravneet Kaur, Sandeep Kr Aggarwal, Mridula Gupta, and R. S. Gupta, Journal of Semiconductor Technology and Science, Vol.10, No.1, 66-77, (March), 2010.
- [197]. “Analytical modeling of Channel noise for Gate Material Engineered Surrounded/Cylindrical Gate (SGT/CGT) MOSFET”, Pujarini Ghosh, Rishu Chaujar, Subhasis Haldar, R.S Gupta and Mridula Gupta, World Academy of Science, Engineering and Technology Journal No.64 (April), 2010.
- [198]. “Microwave performance enhancement in Double and Single Gate HEMT with channel thickness variation”. Ritesh Gupta, Servin Rathi, Mridula Gupta and R S Gupta, Superlattice and Microstructures, Vol. 47, No. 6, P. 779-794, (June) 2010.
- [199]. “An analytical charge-based drain current model for nanoscale In<sub>0.52</sub>Al<sub>0.48</sub>As-In<sub>0.53</sub>Ga<sub>0.47</sub> As separated double-gate HEMT”, Servin Rathi, Jyotika Jogi, R.S. Gupta and Mridula Gupta, Semiconductor Science and Technology, Vol. 25, No.11, P. 115003-115009, (Oct) 2010.
- [200]. “Physics Based Threshold voltage analysis of Gate Material Engineered Trapezoidal Recessed Channel (GME TRC) Nanoscale MOSFET and its Multilayered gate architecture”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S Gupta. International Journal of Microwave and Optical Technology, Vol.5, No.6, P.361-368, (Nov) 2010.
- [201]. “Device linearity and intermodulation distortion comparison of Dual Material Gate and conventional AlGaIn/GaN High Electron Mobility Transistor”, Sona P Kumar,

- Anju Agrawal, Rishu Chaujar, Mridula Gupta and R.S. Gupta. *Microelectronics Reliability*. Vol. 51, No.3, P. 587-596, (March) 2011.
- [202]. “Improved Linearity Performance of AlGa<sub>N</sub>/Ga<sub>N</sub> MISHFET over Conventional HFETs: An Optimization Study for Wireless Infrastructure Applications”, Ruchika Aggarwal, Anju Agrawal, R.S Gupta. and Mridula Gupta. *Superlattice and Microstructures*. Vol.50, No. 1, P.1-13, (July) 2011.
- [203]. “Scattering parameter based Modeling and Simulation of symmetric tied-gate InAlAs/InGaAs DG-HEMT for millimeter-wave applications”, Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta. *Solid State Electronics*, Vol.63, No.1, P.149-153, (September) 2011.
- [204]. “TCAD Assessment of Device Design Technologies for Enhanced Performance of Nanoscale DG MOSFET”, Rupendra Sharma, Mridula Gupta and R.S Gupta, *IEEE Trans. Electron Devices*. Vol. 58, No. 9, P. 2936-2943, (September), 2011.
- [205]. “Linearity-Distortion analysis of GME-TRC MOSFET for High Performance and Wireless Applications”, Priyanka Malik, R.S.Gupta, Rishu Chaujar and Mridula Gupta, *Journal of Semiconductor Technology and Science*, P. 152-174, (July) 2011.
- [206]. “Impact of Interface Fixed Charges on the Performance of the Channel Material Engineered Cylindrical Nanowire MOSFET”, Rajni Gautam, Manoj Saxena, R.S. Gupta, and Mridula Gupta, *AIRCC journal (International journal of VLSI design & Communication Systems VLSICS)*, Vol. 1, No. 3, P. 225-241, (September), 2011.
- [207]. “Linearity and Analog Performance Analysis of Double Gate Tunnel FET: Effect of Temperature and Gate Stack”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta, *International journal of VLSI design & Communication Systems (VLSICS)*, Vol. 2, No. 3, P.185-200, (September), 2011.
- [208]. “AC Analysis of nanoscale GME-TRC MOSFET for Microwave and RF Applications”, Priyanka Malik, R.S.Gupta, Rishu Chaujar and Mridula Gupta. *Microelectronic Reliability*, Vol. 52, no. 1, pp. 151-158 (January), 2012.
- [209]. “An Analytical Drain Current Model for Dual Material Engineered Cylindrical/Surrounded Gate MOSFET”, Pujarini Ghosh, Subhasis Haldar, R.S. Gupta, and Mridula Gupta, *Microelectronics Journal*, Vol. 43, pp.17-24, 2012.
- [210]. “Dielectric Modulated Tunnel Field Effect Transistor – A Bio molecule Sensor” Rakhi Narang, Manoj Saxena, R.S. Gupta, and Mridula Gupta *IEEE Electron Device Letters*, vol. 33, no. 2, pp. 266-268, (Feb) 2012.
- [211]. “Two Dimensional Analytical Subthreshold Model of Nanoscale Cylindrical Surrounding Gate MOSFET Including Impact of Localised Charges”, Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, *Journal of computational and theoretical nanoscience*, Vol.9, No.4, p.602-610. (April) 2012.
- [212]. “Simulation Study of Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET for High Temperature Applications” Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta, *Microelectronics Reliability* Vol.52, No.8, pp.1610:1612 (August), 2012
- [213]. “Gate-Geometric Recessed Nano-scale In<sub>0.52</sub>Al<sub>0.48</sub>As-In<sub>0.53</sub>Ga<sub>0.47</sub>As Double-Gate HEMT for High Breakdown” Servin Rathi, Mridula Gupta and R. S. Gupta, *IEEE Transaction on Device and Material Reliability* Vol. 12, No. 1, pp.139-145, 2012.



- [214]. “Effect of Localised Charges on Nanoscale Cylindrical Surrounding Gate MOSFET: Analog Performance and Linearity Analysis” Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, *Microelectronics Reliability*, vol. 52, no.6, pp. 989-994, (June) 2012.
- [215]. “Immunity against Temperature Variability and Bias point Invariability in Double Gate Tunnel Field Effect Transistor” Rakhi Narang, Manoj Saxena, R.S.Gupta and Mridula Gupta, *Microelectronics Reliability*, Vol.52, No.8, pp.1617-1620. (August) 2012.
- [216]. “Temperature Dependent Drain Current Model for Gate stack Insulated Shallow Extension Silicon on Nothing (ISESON) MOSFET for wide operating temperature range” Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta, *Microelectronics Reliability*. Vol. 52, no. 6, pp. 974–983, June 2012.
- [217]. “An Accurate Charge-Control- Based Approach for Noise Performance Assessment of a Symmetric Tied-Gate INAlAs/InGaAs DG HEMT” Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta, *IEEE Transactions on Electron Devices*, Vol. 59 , no. 6, pp. 1644 – 1652, June 2012.
- [218]. “Two dimensional analytical drain current model for Double Gate MOSFET incorporating Dielectric Pocket (DP-DG)” Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta,. *IEEE Transactions On Electron Devices*, vol 59, no. 10, pp. 2567 - 2574, 2012.
- [219]. “A Dielectric Modulated Tunnel FET based Biosensor for Label Free Detection: Analytical Modeling Study and Sensitivity Analysis.” Rakhi Narang, K. V. S. Reddy, Manoj Saxena, R.S. Gupta, and Mridula Gupta, *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp. 2809-2817, Oct 2012.
- [220]. “Numerical Model of Gate All Around MOSFET With Vacuum Gate Dielectric For Biomolecule Detection”, Rajni Gautam, Manoj Saxena, R.S.Gupta, and Mridula Gupta, *IEEE Electron Device Letters*, vol.33, no.12,pp. 1756-1758,2012
- [221]. “An Accurate Small Signal Modeling of Cylindrical/Surrounded Gate MOSFET for High Frequency Applications” Pujarini Ghosh, Subhasis Haldar, R.S.Gupta and Mridula Gupta. *Journal of Semiconductor Technology and Science* vol 12, No 4 pp-377-387, 2012.
- [222]. “Analytical Modeling and Simulation for Dual Metal Gate Stack Architecture (DMGSA) Cylindrical/Surrounded Gate MOSFET” Pujarini Ghosh, Subhasis Haldar, R.S.Gupta and Mridula Gupta, *Journal of Semiconductor Technology and Science*, Vol.12,no.4, pp. 458-466,2012.
- [223]. “An Investigation of Linearity Performance and Intermodulation Distortion of GME CGT MOSFET for RFIC Design” Pujarini Ghosh, Subhasis Haldar, R.S.Gupta and Mridula Gupta. *IEEE Transactions on Electron Devices*, Vol.59 No. 12 pp. 3263-3268, 2012.
- [224]. “Assessment of Ambipolar Behavior of a Tunnel FET and Influence of Structural Modifications”, Rakhi Narang, Manoj Saxena, R.S. Gupta, and Mridula Gupta, *Journal of Semiconductor Technology and Science*, Vol.12, no.4, pp.482-491, 2012.
- [225]. “Analog and Digital Performance Assessment of Empty Space in Double Gate (ESDG) MOSFET: A Novel Device Architecture”, Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta, *Journal of computational and theoretical nanoscience*

- (JCTN), Vol.10, no. 2, pp.389-398, 2013.
- [226]. "Analytical Model for Double-Gate Tunneling Field-Effect Transistor (DG-TFET) using carrier concentration approach" Rakhi Narang, Manoj Saxena, R.S. Gupta, and Mridula Gupta, Journal of Computational and Theoretical Nanoscience (JCTN), Vol.10, no.5, pp.1-7, 2013.
- [227]. "Numerical analysis of localised charges impact on Static and Dynamic Performance of Nanoscale Cylindrical Surrounding Gate MOSFET Based CMOS Inverter", Rajni Gautam, Manoj Saxena, R. S. Gupta, and Mridula Gupta, Microelectronics Reliability, Vol. 53, Issue2, pp. 236-244, (Feb) 2013.
- [228]. "Investigation of Empty Space in Nanoscale Double Gate (ESDG) MOSFET for High Speed Digital Circuit Applications", Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta, Journal of Semiconductor Technology and Science, Vol. 13, no. 2, pp.127-138, (April) 2013.
- [229]. "Device and Circuit Level Performance Comparison of Tunnel FET Architectures and Impact of Heterogeneous Gate Dielectric", Rakhi Narang, Manoj Saxena, R.S. Gupta, and Mridula Gupta, Journal of Semiconductor Technology and Science, Vol. 13, no.3, pp. 224-236, (June) 2013.
- [230]. "Hot Carrier Reliability of gate All Around MOSFET for RF/Microwave Applications", Rajni Gautam, Manoj Saxena, R.S. Gupta, and Mridula Gupta, IEEE Transactions on Device and Materials Reliability, Vol.13, No. 1, pp 245-251, (March) 2013.
- [231]. "Temperature Dependent Analytical Model for Microwave and Noise Performance Characterization of  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_m\text{Ga}_{1-m}\text{As}$  ( $0.53 \leq m \leq 0.8$ ) DG-HEMT", Monika Bhattacharya, Jyotika Jogi, Mridula Gupta, R.S Gupta, IEEE Transactions on Device and Materials Reliability, Vol. 13, No. 1, pp. 293-300, (March) 2013.
- [232]. "Gate-to-Drain Capacitance Dependent Model for Noise Performance Evaluation of InAlAs/InGaAs Double-gate HEMT", Monika Bhattacharya, Jyotika Jogi, R.S. Gupta and Mridula Gupta, Journal of Semiconductor Technology and Science, Vol.13, No.4, pp. 331-341, (August) 2013.
- [233]. "Quantum Modeling of Nanoscale Symmetric Double Gate InAlAs/InGaAs/InP HEMT" Neha Verma, Mridula Gupta, R.S. Gupta and Jyotika Jogi. Journal of Semiconductor Technology and Science, Vol.13, No.4, pp. 342-354, (August) 2013.
- [234]. "Gate All Around MOSFET with Vacuum Gate Dielectric for Improved Hot Carrier Reliability and RF performance" Rajni Gautam, Manoj Saxena, R.S. Gupta and Mridula Gupta, IEEE Transactions on Electron Devices, Vol. 60, No. 6, pp. 1820-1827, (June) 2013.
- [235]. "Drain Current Model for a Gate All Around (GAA) p-n-p-n Tunnel FET" Rakhi Narang, Manoj Saxena, R.S. Gupta, and Mridula Gupta, Microelectronics Journal, Vol. 44, no.6, pp.479-488, (May) 2013.
- [236]. "RF Characterization of 100nm Separate Gate InAlAs/InGaAs DG-HEMT," Praveen, Mridula Gupta, R.S. Gupta and Jyotika Jogi, Microwave and Optical Technology Letters, Vol. 55, Issue 11, 2796-2803, (November) 2013.
- [237]. "Circuit Level Implementation for Insulated Shallow Extension Silicon on Nothing (ISE-SON) MOSFET : A Novel Architecture", Vandana Kumari, Manoj Saxena, Radhey Shyam Gupta and Mridula Gupta, IETEJR, Vol 59, no.4, pp. 353-359,

- (August) 2013.
- [238]. "Analytical Model of Double Gate MOSFET for high Sensitivity Low Power Photosensor" Rajni Gautam, Manoj Saxena, R.S. Gupta and Mridula Gupta, JSTS, VOL.13, NO.5, (October) 2013.
- [239]. "Performance Investigation of Insulated Shallow Extension Silicon on Nothing (ISE-SON) MOSFET for Low Voltage Digital Applications," Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta, JSTS VOL.13, NO.6, (December) 2013.
- [240]. "Comparative Study of Silicon on Nothing and III-V on Nothing Architecture for high speed and Low Power Analog and RF/Digital Applications," Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta, IEEE Transactions on Nanotechnology, Vol. 12, no.6, pp. 978-984, (Nov) 2013.
- [241]. "Impact of temperature variations on the Device and circuit Performance of tunnel FET:A Simulaion Study," Rakhi Narang, Manoj Saxena, R.S. Gupta and Mridula Gupta, IEEE Transactions on Nanotechnology, Vol. 12, no.6, pp.951-957, Nov 2013.
- [242]. "Gate All Around MOSFET With Catalytic Metal Gate for Gas Sensing Applications," Rajni Gautam, Manoj Saxena, R.S. Gupta and Mridula Gupta, IEEE Transaction on Nanotechnology, Vol. 12, no.6, pp. 939-944, Nov 2013.
- [243]. "Impact of temperature and indium composition in the channel on the Microwave performance of single-gate and double-gate InAlAs/InGaAs HEMT," Monika Bhattacharya, Jytotika Jogi, R.S. Gupta and Mridula Gupta, IEEE Transaction on Nanotechnology, Vol. 12, no.6, pp. 965-970, Nov 2013.
- [244]. "Analytical Modeling of Dielectric Pocket Double Gate (DP-DG) MOSFET Incorporating Hot Carrier Induced Interface Charges,"Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta, IEEE Transactions on Electron Devices Vol. 14, Issue 1, pp. 390 - 399, (March) 2014.
- [245]. "Temperature Dependent Subthreshold Model of Long Channel GAA MOSFET Including Localized Charges to Study Variations in its Temperature Sensitivity," Rajni Gautam, Manoj Saxena, R.S. Gupta and Mridula Gupta, Microelectronics Reliability, Volume 54, Issue 1, Pages 37–43, (January) 2014.
- [246]. "Performance evaluation and reliablity issue of junctionless CSG MOSFET for RFIC design", Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, IEEE Transaction on Device and Material Realibility, Vol. 14, Issue 1, pp. 418-425, March 2014.
- [247]. "An Analytical Subthreshold current modeling of cylindrical Gate All Around(CGAA) MOSFET incorporating the infulence of device design engineering", Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, Microelectronics Journal, Issue 45, pp. 408-415, March 2014.
- [248]. "A New T-Shaped Source/Drain Extension (T-SSDE) Gate Underlap GAA MOSFET with Enhanced Subthreshold Analog/RF Performance for Low Power Applications", Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Solid State Electronics Journal, Volume 101, pp.13–17, (November) 2014.
- [249]. "Impact of Gate Material Engineering(GME) on Analog/RF Performance of Nanowire Schottky-Barrier Gate All Around (GAA) MOSFET for Low Power Wireless applications: 3D T-C AD Simulation", Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Microelectronics Journal. Volume 45, Issue 11, pp. 1508–1514 , (November) 2014.

- [250]. "Influence of Heterogeneous Gate Dielectric on Hetero-Dielectric-DMG-GAATFET for improved tunneling current," Jaya Madan, R.S Gupta, Rishu Chaujar, International Journal of Advanced Technology in Engineering and Science, 2(1), September 2014, pp.-41-47.
- [251]. "Analytical Drain Current Formulation for Gate Dielectric Engineered Dual Material Gate-Gate All Around-Tunneling Field Effect Transistor," Jaya Madan, R.S Gupta, Rishu Chaujar, Japanese Journal of Applied Physics (JJAP), Volume 54, no. 9 August 2015. (In press)
- [252]. "Localised Charge Dependent Threshold Voltage Analysis of Gate Material Engineered Junctionless Nanowire Transistor," Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, IEEE Transactions on Electron Device, Vol. 62, no. 8, pp. 2598-2605, (August) 2015.
- [253]. "Capacitance Modeling of Gate Material Engineered Cylindrical/Surrounded Gate MOSFETs for Sensor Applications," Jay Hind Kumar Verma, Yogesh Pratap, Subhasis Haldar, R. S. Gupta and Mridula Gupta, Superlattices and Microstructures Journal, Volume 88, pp. 271–280, (December) 2015.
- [254]. "Modeling and Simulation of Cylindrical Surrounding Double Gate MOSFET for Enhanced Electrostatic Integrity," Jay Hind Kumar Verma, Subhasis Haldar, R. S. Gupta and Mridula Gupta Superlattices and Microstructures Journal vol. 88, pp 354-364, Dec 2015.
- [255]. "DS-Schottky Barrier Cylindrical GAA MOSFET: Nanosensor for Biochips," Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Nanomaterials and Energy Journal, vol. 5, issue 1, Jan. 2016.
- [256]. "Analytical Modeling of Junctionless Accumulation Mode Cylindrical Surrounding Gate MOSFET (JAM-CSG)", International Journal of Numerical Modelling, Nitin Trivedi, Manoj Kumar, Subhasis Haldar, S. S. Deswal, and R.S. Gupta, DOI: 10.1002/jnm.2162, 2016.
- [257]. "Numerical Modeling of Subthreshold Region of Junctionless Double Surrounding Gate MOSFET (JD SG) ," Sonam Rewari, Subhasis Haldar, , Vandana Nath, S.S. Deswal, and R.S. Gupta. Superlattices and Microstructures Journal, vol. 90, pp 8-19, Dec 2015.
- [258]. " Physics based analytical model for surface potential and subthreshold current of cylindrical schottky barrier Gate All Around MOSFET with High-k Gate stack", Manoj Kumar, Subhasis Haldar, Mridula Gupta, and R.S. Gupta. Superlattices and Microstructures Journal, vol. 90, pp 215-226, Jan. 2016.
- [259]. "Physics-based drain current modeling of gate-all-around junctionless nanowire twin-gate transistor (JN-TGT) for digital applications", Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, Journal of Computational Electronics, 10.1007/s10825-016-0798-1, pp 1-10, 2016.

## II. Papers in International Conference

- [1]. "A new composite transistor in circuit theory SSCT - 74", R.S. Gupta, Academy of Sciences Czechoslovakia, 1974.
- [2]. "Increasing the barrier height of triangular barrier diodes for the use as photovoltaic applications", R.S. Gupta, G.S. Chilana, Third International Conference on the Physics of Semiconductor Devices (IIT Madras), 1985.
- [3]. "New methods to determine the sub-micrometer MOSFET parameters", R.S. Gupta, G.S. Chilana, R. Sood & Alka Nagpal, Inter. Conference and Intensive Tutorial Course on Semiconductor Materials, Dec. 8-16, 1988, New Delhi.
- [4]. "Solar Cell Minority Carrier Life Time Measurement", R.S. Gupta, Alka Nagpal, G.S. Chilana, V.K. Jain & G.P. Srivastava, International Conference and Intensive Course on Semiconductor Materials, December 8-16, 1988, New Delhi.
- [5]. "Characteristics of Modified p-i-n amorphous Silicon Solar Cell", R.S. Gupta, Alka Nagpal, G.P. Srivastava, Fifth International Workshop on Physics of Semiconductor Devices, Dec. 11-15, 1989.
- [6]. "Maximum Threshold Voltage and Extraction of Various Parameters in Sub-micron MOSFETs", R.S. Gupta, Subhasis Haldar & S.K. Dwivedi, 6th International Workshop on Physics of Semiconductor Devices, December 2-6, 1991.
- [7]. "Threshold voltage shift in Depletion Model IGFET", R.S. Gupta, Subhasis Haldar, M.K. Khanna & Maneesha, Third International Conference on Solid State and Integrated Circuit Technology, Beijing, China, October, 1992.
- [8]. "Drain Induced Barrier Lowering and Sub-Threshold Current Model of GaAs MESFET's for Microwave Applications", R.S. Gupta & Rachna Sood, 4th International Symposium on Recent Advances in Microwave Technology, New Delhi, December 15-18, 1993.
- [9]. "Modeling of Ion Implanted Silicon MESFET with three moment approach", R.S. Gupta and Subhasis Haldar, 4th International Symposium on Recent Advances in Microwave Technology, New Delhi, December 15-18, 1993.
- [10]. "Two Dimensional Numerical Analysis for Short Channel GaAs MESFET's with nonuniformly Doped Channel using Perturbation method", R.S. Gupta, Proceeding Asia Pacific Microwave Conference, Taiwan, Vol.2, p.15-20, 18-21 October, 1993.
- [11]. "The effect of Pearson IV distribution on MESFET Intrinsic Gate-source capacitance", R.S. Gupta and S. Rajesh, 5th International Symposium on Recent Advances in Microwave, Kiev, Ukraine, (Invited paper) 1995.
- [12]. "A 2D Analytical Model of GaAs MESFET for high speed circuits applications", R.S. Gupta, progress in Electromagnetic Research Symposium, Washington, USA, (Invited paper) 1995.
- [13]. "A New Analytical MOSFET model for VLSI", R.S. Gupta, Ciby Thomas and S. Haldar, Physics of semiconductor devices, Narosa Publishing House, p. 60-62, 1995.

- [14]. “*New Threshold Voltage Model for an Ion Implanted GaAs MESFET*,” R.S. Gupta, Y.D. Sharma, Ciby Thomas, Physics of semiconductor devices, Narosa Publishing House, p. 138-140, 1995.
- [15]. “*Submicrometer GaAs MESFET Modeling using trial function approach*”, R.S. Gupta and Sunita A. Chhokra, Asia-Pacific Microwave Conference (APMC’96), New Delhi, December 17-20, 1996.
- [16]. “*Influence of FMA on the switching characteristics of ion-implanted Si FETs under thermal annealing*”, R.S. Gupta, S. Rajesh, Asia-Pacific Microwave Conference (APMC’96), New Delhi, December. 17 - 20, 1996.
- [17]. “*A model for short channel polycrystalline-silicon thin-film transistor for microwave applications*”, R.S. Gupta and Sonia Chopra, Asia-Pacific Microwave Conference (APMC’96), New Delhi, December 17-20, 1996.
- [18]. “*Study of DIBL in short channel MOSFET*”, R.S. Gupta & Manju Pruthi, Asia-Pacific Microwave Conference (APMC’96), New Delhi, December 17-20, 1996.
- [19]. “*Lightly doped drain (LDD) MOSFETs: An optimized model for very high cut off frequencies*” R.S. Gupta, Ciby Thomas, S. Haldar, M.K. Khanna, & Maneesha, APMC’96, New Delhi, December 17-20, 1996.
- [20]. “*Bandgap discontinuity dependent model for 2-DEG density at the AlGaAs/GaAs interface*”, R.S. Gupta, Sujata Sen and Manoj K. Pandey, Asia-Pacific Microwave Conference (APMC’96), New Delhi, December 17-20, 1996.
- [21]. “*Temperature dependence on threshold voltage and drain current in thin film SOI OSFETs*”, R.S. Gupta, Prasenjeet Bose, Subhasis Haldar, S. Rajesh, and Ciby Thomas, Asia-Pacific Microwave Conference (APMC’96), New Delhi, December 17 - 20, 1996.
- [22]. “*Back bias dependence of I-V characteristics of a fully depleted double gate SOI MOSFET*”, R.S. Gupta, Manoj K. Panday, Sujata Sen and S Rajesh, Asia-Pacific Microwave Conference (APMC’96), New Delhi, December 17-20, 1996.
- [23]. “*Analytical Modeling of Device Conductances of Lightly Doped Drain (LDD) MOSFETs*”, R.S. Gupta, Ciby Thomas, Subhasis Haldar, Manoj K. Khanna, 21<sup>st</sup> International Conference on Microelectronics, to be held in Nis, Yugoslavia, 15 – 17 Sept. 1997.
- [24]. “*A Quasi Two-Dimensional Analytical Model for Threshold Voltage of a Modulation Doped Field Effect Transistor*”, R.S. Gupta, Sujata Sen, Manoj Panday, Manoj Khanna, Asia-Pacific Microwave Conference (APMC’97), to held in Hong Kong SAR, PRC, Dec. 2-5, 1997.
- [25]. “*A Fringing Capacitance Based Cut Off Frequency Model for Lightly Doped Drain (LDD) MOSFETs*”, R.S. Gupta, Ciby Thomas, Int. Symposium on Recent Advances in Microwave Technology (ISRAMT ’97), China, 1997.

- [26]. “*Optimisation of High Performance Fully Overlapped LDD (FOLD) MOSFETs*” R.S. Gupta, Ciby Thomas, Manoj Khanna, S. Haldar, International Workshop on Physics of Semiconductor Devices, New Delhi, India, 1997.
- [27]. “*Current Saturation and Small Signal Characteristics of Non-Self Aligned GaAs MESFET*”, R.S. Gupta, Sunita A Chhokra, 5th International Conference on VLSI and CAD, to be held in Seoul, Korea, Oct. 13-15, 1997.
- [28]. “*A New Analytical 2-D Potential Distribution Model in Subthreshold Region Including DIBL in Short Channel MOSFET*” R.S. Gupta, Manju Pruthi, International Workshop on Physics of Semiconductor Devices, New Delhi, India, 1997.
- [29]. “*A New Capacitance Model for Narrow Channel Depletion Mode MOSFETs*” Subhais Haldar, M.K. Khanna, Ciby Thomas and R.S. Gupta, International Conference on Computer and Devices for Communication (CODEC), Calcutta, January 14-17, 1998.
- [30]. “*A Two-Dimensional I-V Model for Frequency Optimization of Heterostructure Field Effect Transistor (FET)*, Sujata Sen, Manoj K. Khanna and R.S. Gupta, International Conference on Computer and Devices for Communication (CODEC), Calcutta, January 14-17, 1998.
- [31]. “*2-D Potential Distribution Model for Short Channel n-MOSFET with Gaussian Doping*” Manju Pruthi and R.S. Gupta, International Conference on Computer and Devices for Communication (CODEC), Calcutta, January 14-17, 1998.
- [32]. “*Temperature and Scattering Mechanism Dependent Characteristics of an Ionimplanted GaAs OPFET*” Srikanta Bose and R.S. Gupta, International Conference on Photonics-98, IIT Delhi, New Delhi, India, Pp. 739-742, Dec. 14-18, 1998.
- [33]. “*Modelling of Pseudomorphic Modulation Doped Field Effect Transistor (AlGaAs/InGaAs) for Microwave and Millimeter Wave Applications*”, Anju Agrawal, Anisha Goswami and R.S. Gupta, 3rd International Conference on LDSD, Turkey, September 15-17, 1999.
- [34]. “*High Frequency Y-Parameters Analysis of Small Geometry MOSFET for Microwave Frequency Applications*”, Anisha Goswami, Anju Agrawal, S. Haldar, Mridula Gupta and R.S. Gupta, International Symposium on Recent Advances in Microwave Technology (ISRAMT), Vol. 1, Pp. 125-129, December 1999.
- [35]. “*Fringing Field Dependent Small Geometry MOSFET Model for Radio Frequency Applications*”, Anisha Goswami, Subhais Haldar, Mridula Gupta and R.S. Gupta, Tenth International Workshop on Physics of Semiconductor Devices, Vol. 1, Pp. 568- 571, New Delhi, December 14-18, 1999.
- [36]. “*Semi-Empirical Model to Predict the Threshold Voltage and Id-Vd Characteristics of Short Geometry LDD MOSFETs*”, Ekta Kalra, Anil Kumar, Subhais Haldar and R.S. Gupta, Tenth International Workshop on Physics of Semiconductor Devices, New Delhi, Vol. 1, Pp. 594-597, December 14-18, 1999.
- [37]. “*An Analytical Temperature Dependent Threshold Voltage Model for Thin Film Surrounded Gate SOI MOSFET*”, Abinav Kranti, Subhais Haldar and R.S. Gupta, Tenth International Workshop on Physics of Semiconductor Devices, Vol. 1, Pp. 605- 608, New Delhi, December 14-18, 1999.

[38]. "A Model for the Subthreshold Behavior of Short Channel Poly-Si TFT", Sonia Chopra and R.S. Gupta, Tenth International Workshop on Physics of Semiconductor Devices, New Delhi, Vol. 1, 829-832, December 14-18, 1999.

[39]. "Fringing Capacitance and Parasitic Resistance Dependant characteristics of Fully Overlapped Lightly Doped Drain MOSFET", Anil Kumar, Ekta Kalra, Subhasis Haldar and R.S. Gupta, Tenth International Workshop on Physics of Semiconductor Devices, New Delhi, Vol. 1, Pp. 621-624, December 14-18, 1999.

[40]. "Analytical Model for Field distribution and Capacitance-Voltage characteristics of Pseudomorphic (AlGaAs/InGaAs) Modulation Doped Field Effect Transistor", Anju Agarwal, Sujata Sen and R.S. Gupta, Tenth International Workshop on Physics of Semiconductor Devices, New Delhi, Vol. 1, Pp. 542-545, Dec. 14-18, 1999.

[41]. "Analytical modeling of threshold voltage and drain current in short channel fully depleted cylindrical gate MOSFET", R.S. Gupta, Abhinav Kranti and S. Haldar, Tenth International Workshop on Physics of Semiconductor Devices, New Delhi, Vol. 1, Pp. 475-482, December 14-18, 1999.

[42]. "Modeling of current voltage characteristics of modulation doped field effect transistor with velocity overshoot effect" Sujata Sen, Manoj K. Panday and R.S. Gupta, Tenth International Workshop on Physics of Semiconductor Devices, New Delhi, Vol. 1, Pp. 651-654, December 14-18, 1999.

[43]. "DC and microwave performance of pseudomorphic modulation doped field effect transistor (AlGaAs/InGaAs) for millimeter wave and high speed digital IC applications", Anju Agrawal, Anisha Goswami and R.S. Gupta, In Proc. XIIth Asia Pacific Microwave Conference, Sydney Australia, pp. 144-148, December 3-6, 2000.

[44]. "A two-dimensional analytical model for thin film fully depleted surrounding gate (SGT) MOSFET", Abhinav Kranti, S. Haldar and R.S. Gupta, In Proc. XIIth Asia Pacific Microwave Conference, Sydney Australia, pp. 880-883, Dec. 3-6, 2000.

[45]. "A threshold voltage model for short channel GaAs OPFET for optical communication system", S. Bose, Mridula Gupta and R.S. Gupta, In Proc. XIIth Asia Pacific Microwave Conference, Sydney Australia, pp. 1077-1080, December 3-6, 2000.

[46]. "A new threshold voltage model for short channel GaAs OPFET for optical communication systems" S. Bose, and R.S. Gupta, PIERS'2000, Pp. 52, 2000.

[47]. "Admittance parameter extraction of short gate length MOSFET including substrate effect for microwave frequency applications", A. Goswami, A. Agarwal, M. Gupta and R.S. Gupta, PIERS'2000, Pp. 1060, 2000.

[48]. "Photo effect Id-Vd characteristics of non-self aligned short channel GaAs MESFET", S. Bose, M. Gupta and R.S. Gupta, Photonics' 2000, Vol. 2, Pp. 738-740, Calcutta, December 18-20, 2000.



- [49]. “*Analytical model for optically controlled fully depleted cylindrical surrounding gate (CGT/SGT) MOSFET*”, Abhinav Kranti, S. Haldar and R.S. Gupta, *Photonics*’ 2000, Vol. 2, Pp. 590-592, Calcutta, December 18-20, 2000.
- [50]. “*Design guidelines of vertical surrounding gate (VSG) MOSFETs for future ULSI circuit applications*”, Abhinav Kranti, Rashmi, S. Haldar and R.S. Gupta, Topical Meeting on Silicon Monolithic Integrated circuits in RF systems, Ann Arbor, Michigan, U.S.A., September 12-14, 2001.
- [51]. “*Analytical approach to evaluate unilateral power gain of optically biased GaAs MESFET*” Srikanta Bose, Mridula Gupta and R.S. Gupta, PIERS’ 2001, Osaka, Japan, July 18-22, 2001.
- [52]. “*A new model for lattice matched InAlAs/InGaAs/InP HEMT for microwave applications*”, Jyotika Jogi, Mridula Gupta and R.S. Gupta, 8th International Symposium on Microwave and Optical Technology, Montreal, Canada, June 20-24, 2001.
- [53]. “*An analytical approach to evaluate 1/f noise of fully overlapped lightly doped drain MOSFETs*”, Anil Kumar, Ekta Kalra, S. Haldar, R.S. Gupta, International Conference on Noise in Physical Systems and 1/f Fluctuations, Gainesville, Florida, USA, October 2001.
- [54]. “*Piezoelectric polarization dependent model of AlGaIn/GaN high electron mobility transistors for improved microwave performance*”, Rashmi, A Kranti, S Haldar and R S Gupta, Asia Pacific Microwave Conference, Taipei, Taiwan, R.O.C., December 3-6, 2001.
- [55]. “*Analytical model for DC characteristics of GaN MESFET Under Dark and illuminated Conditions*”, Adarsh, Srikanta Bose, Mridula Gupta and R S Gupta, Asia Pacific Microwave Conference, Taipei, Taiwan, R.O.C., Dec. 3-6, 2001.
- [56]. “*Analytical Modeling of Polysilicon TFT Using Charge Sheet Approach*” Simrata Bindra, Subhasis Haldar and R S Gupta, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 1, p. 632-636, December 11-15, 2001 at IIT Delhi, India.
- [57]. “*Analytical Model for C~V Characteristics of GaN MESFET for Microwave Frequency Applications*” Adarsh, Srikanta Bose, Mridula Gupta and R. S Gupta, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 2, p. 846-849, December 11-15, 2001 at IIT Delhi, India.
- [58]. “*Saturation Drain Current and Substrate Current Model of Fully Overlapped LDD MOSFET*” Anil Kumar, Ekta Kalra, Subhasis Haldar and R S Gupta, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 2, p. 1429-1432, December 11-15, 2001 at IIT Delhi, India.
- [59]. “*A Physics Based Charge Control Model of Lattice Mismatched AlGaIn/GaN HEMTs*” Rashmi, A Kranti, S Haldar and R S Gupta, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 2, p. 911-914, December 11-15, 2001 at IIT Delhi, India.

[60]. “*Threshold Voltage Model for Short Channel Retrograde Doped MOSFETs*” Abhinav Kranti, Rashmi, S Haldar and R S Gupta, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 1, p. 672-676, December 11-15, 2001 at IIT Delhi, India.

[61]. “*An Accurate Model for Planar Doped InAlAs/InGaAs/InP MODFETs for Microwave Circuit Applications*” Ritesh Gupta, Abhinav Kranti, S. Haldar, Mridula Gupta and R.S. Gupta, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 2, p. 865-869, December 11-15, 2001 at IIT Delhi, India.

[62]. *Modeling of current-voltage characteristics and Transconductance of Extrinsic Lattice Matched InAlAs/InGaAs/InP HEMT for Very High Frequency Application*”, Jyotika Jogi, Mridula Gupta, and R.S. Gupta, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 2, p. 870-873, December 11-15, 2001 at IIT Delhi, India.

[63]. “*Modeling of Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN Heterostructure Field Effect Transistors (HFETs) for Microwave and Millimeter Wave Circuit Applications (Invited)*” R S Gupta, Rashmi, A Kranti and Subhasis Haldar, Eleventh International Workshop on Physics of Semiconductor Devices, (IWPSD-2001), Vol. 2, p. 819-826, December 11-15, 2001 at IIT Delhi, India.

[64]. “*Simultaneous effect of optical radiation, temperature hydrostatic pressure on GaAs based device parameters*”, Srikanta Bose, Mridula Gupta, R.S. Gupta and C.L. Pan, Progress in Electromagnetics Research Symposium, (PIERS’2002), Cambridge, Massachusetts, USA, July 1-5, 2002.

[65]. “*Closed form Analytical Threshold Voltage Model of Dual Material Double-gate (DUM-DG) MOSFET*” R. S. Gupta, Manoj Saxena and Mridula Gupta, Asia-Pacific Microwave Conference – (APMC-2003), South Korea.

[66]. “*Optimization of InAlAs/InGaAs heterostructure, InP based HEMT for its microwave frequency applications*” R.S. Gupta, Ritesh Gupta and Mridula Gupta, 9th International Symposium on Microwave and Optical Technology, Ostrava, Czech Republic, August 11-15, 2003.

[67]. “*Temperature dependent characterization of InAlAs/InGaAs/InP LMHEMT for microwave frequency application*” Jyotika Jogi, Sujata Panday and R.S. Gupta, 9th International Symposium on Microwave and Optical Technology (ISMOT-2003), Ostrava, Czech Republic, August 11-15, 2003.

[68]. “*Lattice Temperature Dependent Thermal Noise Model Using Distributed Gate Structure for RF Applications*” Nirupama Kapoor, Subhasis Haldar, Mridula Gupta and R S Gupta, proceedings of the 12th International Workshop on Physics of Semiconductor Devices, IIT, Madras, India, December 16-20, 2003

[69]. “*Noise Modelling of MODFET Based on Accurate Charge Control Model*” R.S. Gupta, Mridula Gupta, Vandana Guru and H.P. Vyas, proceedings of the 12th International Workshop on Physics of Semiconductor Devices, IIT, Madras, Dec.16-20, 2003.

- [70]. “*Characterization and Analysis of Poly-Si TFTs in the Saturation Region*” Simrata Bindra, Subhasis Haldar and R.S. Gupta, proceedings of the 12th International Workshop on Physics of Semiconductor Devices, IIT, Madras, India, Dec. 16-20, 2003.
- [71]. “*Model design and analysis of temperature and Al composition dependent transport properties of submicron AlGaAs/GaAs HEMTs: a new approach*” Sujata Pandey, Manoj Pandey, Rajesh Tyagi, Jyotika Jogi and R.S. Gupta, proceedings of the 12th International Workshop on Physics of Semiconductor Devices, IIT, Madras, India, December 16-20, 2003.
- [72]. “*Effect of Implantation Profile on Design Aspects of Double Gate SOI-MOSFET*” Manoj K Pandey, Sujata Pandey, Alok Khushwaha, R.S. Gupta, proceedings of the 12th International Workshop on Physics of Semiconductor Devices, IIT, Madras, India, December 16-20, 2003.
- [73]. “*Analytical Model of Non-self aligned SiC MESFET*” Sandeep Kumar Aggarwal, Subhasis Haldar, Mridula Gupta and R.S. Gupta, proceedings of the 12th International Workshop on Physics of Semiconductor Devices, IIT, Madras, India, December 16-20, 2003.
- [74]. “*HEMGAS: A Novel Gate Workfunction Engineered Stacked Gate Oxide Concept for Sub-50 nm DG-MOSFET*” Manoj Saxena, Mridula Gupta and R. S. Gupta, International Conference on Computer and Devices for Communication (CODEC-2004), January 1 – 3, Calcutta, 2004.
- [75]. “*Modeling of gate capacitance and cut off frequency of poly-Si thin film transistor*” Simrata Bindra, Subhasis Haldar and R.S. Gupta, International Conference on Computer and Devices for Communication (CODEC-2004), January 1 – 3, Calcutta, 2004.
- [76]. “*Analytical model for non-self aligned buried p-layer SiC MESFET*”, Sandeep K. Aggarwal, Ritesh Gupta, Subhasis Haldar, Mridula Gupta and R.S. Gupta, IEEE Laster Eastman Conference on High Performance Device, Pp. – 112 – 113, 4 – 6, August, New York, 2004.
- [77]. “*Two dimensional analytical modeling and simulation of retrograde doped HMG MOSFET*” R.S. Gupta, K. Goel, M. Saxena and M. Gupta, IEEE Laster Eastman Conference on High Performance Device, Page – 85-86, 4 – 6, August, New York, 2004.
- [78]. “*Two dimensional analytical modeling of fully depleted poly-crystalline silicon thin film transistor*”, Amit Sehgal, Tina Mangla, Mridula Gupta and R.S. Gupta, TFFT VII Symposium, 3-8, October 2004.
- [79]. “*Sub-threshold analysis for poly-silicon thin film transistor using green’s function approach*” Amit Sehgal, Tina Mangla, Mridula Gupta and R.S. Gupta, Asia-Pacific Microwave Conference (APMC’04), New Delhi, India, December 2004.
- [80]. “*Physics Based Modeling and Simulation of Epitaxial Channel Hetero Material Gate Stack (EPI-HEMGAS MOSFET)*” Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, Asia-Pacific Microwave Conference (APMC’04), New Delhi, India, December 2004.

[81]. "Scattering parameters evaluation of GaAs pseudomorphic HEMT", Vandana Guru, H.P. Vyas, Mridula Gupta and R.S. Gupta, Asia-Pacific Microwave Conference (APMC'04), New Delhi, India, December 2004.

[82]. "Analytical Analysis and Simulation of High-K Dielectric in Gate Stack Silicon-On-Nothing (GAS-SON) MOSFET for Sub-100 nm Gate Length", Poonam Kasturi, Manoj Saxena and R.S. Gupta, Asia-Pacific Microwave Conference (APMC'04), New Delhi, India, December 2004.

[83]. "A semi-empirical model for current-voltage characteristics of sub-micron GaN MESFET'S" Sneha Kabra, Mridula Gupta, Subhasis Halder and R.S. Gupta, Asia-Pacific Microwave Conference (APMC'04), New Delhi, India, December 2004.

[84]. "Analysis of thermal noise in fully depleted n-channel", Manoj K. Pandey, Alok Kushwaha, P.J. Goerge, Sujata Pandey and R. S. Gupta, Asia-Pacific Microwave Conference (APMC'04), New Delhi, India, December 2004.

[85]. "Impact of gate stack architecture on MOSFETS including quantum mechanical effects" Tina Mangla, Amit Sehgal, Subhasis Halder and R.S. Gupta, Asia-Pacific Microwave Conference (APMC'04), New Delhi, India, December 2004.

[86]. "Two-Dimensional Analysis and Simulation for Gate Stack Silicon-on-Nothing MOSFET (GAS-SON MOSFET)" Poonam Kasturi, Manoj Saxena, R.S. Gupta, In Proceeding 10th International Symposium on Microwave and Optical Technology (ISMOT-2005) Fukuoka Institute of Technology Japan from August 22-25, 2005.

[87]. "Modeling and Simulation of Poly-Crystalline Silicon Thin Film Transistor for Improved Gate Transport Efficiency" Amit Sehgal, Tina Mangla, Sonia Chopra, Mridula Gupta and R.S. Gupta, In Proceeding 10th International Symposium on Microwave and Optical Technology (ISMOT-2005) Fukuoka Institute of Technology Japan from August 22-25, 2005.

[88]. "Investigating the role of Stacked Gate Oxide and Hetro-Material Gate on Electrical Characteristics of Insulated Shallow Extension (ISE) MOSFET" Ravneet Kaur, Manoj Saxena, and R. S. Gupta, Thirteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2005), NPL, New Delhi, December 13-17, Vol 2, Pp. 1163-1166, 2005.

[89]. "Poly-crystalline silicon thin film transistor: modified Schottky gate contact for enhanced gate transport efficiency" Amit Sehgal, Tina Mangla, Sonia Chopra, Mridula Gupta, R. S. Gupta, Thirteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2005), NPL, New Delhi, December 13-17, Vol 2, Pp. 1040-1044, 2005.

[90]. "Threshold voltage model for short-channel MOSFETs with quantum effects" Tina Mangla, Amit Sehgal, Mridula Gupta and R. S. Gupta, Thirteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2005), NPL, New Delhi, December 13-17, Vol 2, Pp. 1030-1034, 2005.

- [91]. “*An Analytical Two-Dimensional Model for Graded Channel Fully Depleted Cylindrical/Surrounding Gate SOI MOSFETs*”, Harsupreet Kaur, Sneha Kabra, Simrata Bindra, Subhasis Haldar and R.S.Gupta, Thirteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2005), NPL, New Delhi, December 13-17, Vol 2, Pp. 1150-1154, 2005.
- [92]. “*An Analytical Model for I-V characteristics of Sub-micron GaN MESFET Using an Exact Velocity Field Dependence for Microwave Applications*”, Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta and R. S. Gupta, Thirteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2005), NPL, New Delhi, December 13-17, Vol 2, Pp. 826-829, 2005.
- [93]. “*Non-Uniformly Doped Gate Electrode Workfunction Engineered MOSFET: Novel Design Architecture for Controlling Short Channel Effect and Improving Gate Transport Efficiency*”, R. S. Gupta, Kirti Goel, Manoj Saxena, Mridula Gupta, Thirteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2005), NPL, New Delhi, December 13-17, Vol 2, Pp. 995-1002, 2005.
- [94]. “*Effect of temperature on current voltage characteristics of lattice mismatched AlGaIn-mN/GaN HEMTs*” Parvesh, S. Pandey, S. Haldar, Mridula Gupta and R.S. Gupta, Proceedings in Asia Pacific Microwave Conference (APMC'05), China, December 4-7, 2005.
- [95]. “*Physics based modeling and simulation of Hetro material asymmetric Gate epi (HEMAGASE) MOSFET*”, Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, Proceedings in Asia Pacific Microwave Conference (APMC'05), China, December 4-7, 2005.
- [96]. “*Modeling and analysis of graded channel fully depleted cylindrical/surrounding gate SOI MOSFETs*”, Harsupreet Kaur, Sneha Kabra, Simrata Bindra, Subhasis Haldar and R.S. Gupta, XXVIIIth General Assembly of International Union of Radio Science (URSI), New Delhi, India, October 23-29, 2005.
- [97]. “*Temperature Dependent Analytical Model Of 6H-SiC MOSFET*”, Navneet Kaushik, Subhasis Haldar, Mridula Gupta and R. S. Gupta, XXVIIIth General Assembly of International Union of Radio Science (URSI), New Delhi, India, October 23-29, 2005.
- [98]. “*Dual-Material Gate Asymmetric Oxide (DMGASYMOX) Stack MOSFET: A Novel Device Architecture for Improved Carrier Transport Efficiency and Reduced Hot Electron Effects*”, Kirti Goel, Manoj Saxena, Mridula Gupta and R.S.Gupta, XXVIIIth General Assembly of International Union of Radio Science (URSI), New Delhi, India, October 23-29, 2005.
- [99]. “*Three region hetero-material gate oxide stack (TMGOS) epi-MOSFET: A new device structure for reduced short channel effects*” Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, 2005 International Semiconductor Device Research Symposium (ISDRS-2005), Holiday Inn Select, Bethesda Maryland, USA December 7-9, 2005.
- [100]. “*Comparison of Three Region Multiple Gate Nanoscale Structures for Reduced Short Channel Effects and High Device Reliability*”, Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, Workshop on Compact Modeling (WCM 06), May 9-11, 2006, Boston, Massachusetts, U.S.A.

[101]. “*An analytical threshold voltage model for sub-micron GaN MESFET*” Sneha Kabra, Hasupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S. Gupta, European Workshop on III Nitride Semiconductors Materials and Devices (EW3NS), Anissaras Hersonissos, Heraklion, Crete, Greece, September 18-20, 2006.

[102]. “*An analysis of bias dependent performance of AlGaIn/GaN High Electron Mobility transistor using new velocity-field dependence*” Sona P Kumar, Anju Agrawal, Sneha Kabra, Mridula Gupta and R.S. Gupta, European Workshop on III Nitride Semiconductors Materials and Devices (EW3NS), Anissaras Hersonissos, Heraklion, Crete, Greece, September 18-20, 2006.

[103]. “*An analytical model for high temperature operation of GaN MESFETs*” Sneha Kabra, Hasupreet Kaur, Subhasis Haldar, Mridula Gupta and R.S. Gupta, International Conference on Computer and Devices for Communication (CODEC-2006), December 18-21, Calcutta, 2006.

[104]. “*Gate Oxide Engineered Dual Material Gate Insulated Shallow Extension (GOXDMG-ISE) MOSFET: A New Vent to Wireless Communication*”, Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R.S. Gupta, International Conference on Computer and Devices for Communication (CODEC-2006), P. 324-327, December 18-21, Calcutta, 2006.

[105]. “*Exploration of the Effect of Negative Junction Depth on Electrical Characteristics of Concave DMG MOSFET in Sub-50 Nanometer Regime*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, International Conference on Computer and Devices for Communication (CODEC-2006), December 18-21, Calcutta, 2006.

[106]. “*An Analytical model for Various Gate Geometries (N, L, F and T-gate) of SOI SiC MESFET*” Sandeep Kr Aggarwal, Ritesh Gupta, Mridula Gupta and R. S. Gupta, International Conference on Computer and Devices for Communication (CODEC-2006), December 18-21, Calcutta, 2006.

[107]. “*Physics based threshold voltage extraction and simulation for double-gate sub-100 nm MOSFETs*” Amit Sehgal, Tina Mangla, Mridula Gupta, R. S. Gupta, (ICMAT 2007) International Conference on Materials for Advanced Technologies 2007, Singapore, 2007.

[108]. “*Nanoscale insulated shallow extension MOSFET with dual material gate for high performance analog operations*” Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.

[109]. “*Performance consideration of a novel architecture: ISEGaS deca-nanometer MOSFET*”, Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.

[110]. “*Laterally asymmetric channel gate stack (LACGAS) SGT: A new structural concept for improved device performance*”, Hasupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.

- [111]. *"A two-dimensional analytical model for I-V characteristics for graded channel surrounding gate (GC SGT) MOSFET"*, Harsupreet Kaur, Sneha Kabra, Subhasis Halder and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.
- [112]. *"RF-Distortion in Sub-100nm L-DUMGAC MOSFET"* Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.
- [113]. *"Two-dimensional analytical threshold voltage model for nanoscale SG-Concave MOSFET in sub-50nm regime"*, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.
- [114]. *3-Dimensional analytical modeling and simulation of fully depleted AlGaIn/GaN modulation doped field effect transistor"*, Sona P. Kumar, Rishu Chaujar, Mridula Gupta and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.
- [115]. *"Influence of physical parameters & piezoelectric polarization on charge control characteristics of Siz Ny/AlGaIn/GaN metal insulator semiconductor heterostructure field effect transistor (MISHFET)"*, Ruchika Aggarwal, Anju Agrawal, Mridula Gupta and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.
- [116]. *"A 2-D analytical subthreshold model for gate misalignment effect on graded channel DG FD SOI n-MOSFET"*, Rupendra Kumar Sharma, Manoj Saxena, Mridula Gupta and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.
- [117]. *"An analytical model for admittance parameters of GaN MESFET for microwave circuit applications"*, Sneha Kabra, Harsupreet Kaur, Subhais Halder, Mridula Gupta and R.S. Gupta, Fourteenth International Workshop on the Physics of Semiconductor Devices (IWPSD-2007), December 16-20, 2007, Mumbai.
- [118]. *"Linearity assessment in DMG ISEGaS MOSFET for RFIC Design"* Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R.S. Gupta, Nineteenth Asia Pacific Microwave Conference (APMC-2007), December 11-14, 2007, Bangkok, Thailand.
- [119]. *"Analytical Modeling and Simulation of Potential and Electric Field Distribution in Dual Material Gate HEMT For Suppressed Short Channel Effects"*, Sona P. Kumar, Rishu Chaujar, Mridula Gupta and R.S. Gupta, Nineteenth Asia Pacific Microwave Conference (APMC-2007), December 11-14, 2007, Bangkok, Thailand.
- [120]. *"Asymmetric gate stack surrounding gate transistor (ASYMGAS SGT): 2-D analytical threshold voltage model"*, Harsupreet Kaur, Sneha Kabra, Subhasis Halder and R.S. Gupta, Nineteenth Asia Pacific Microwave Conference (APMC-2007), December 11-14, 2007, Bangkok, Thailand.

- [121]. "An analytical drain current model for AlGa<sub>N</sub>/Ga<sub>N</sub> metal insulator semiconductor heterostructure field effect transistor (MISHFET): A comparative study with conventional HFETs for high power microwave applications", Ruchika Aggarwal, Anju Agrawal, Mridula Gupta and R.S. Gupta, Nineteenth Asia Pacific Microwave Conference (APMC-2007), December 11-14, 2007, Bangkok, Thailand.
- [122]. "Two-Dimensional Simulation of C-V Characteristics of Deep Submicron Al<sub>m</sub>Ga<sub>1-m</sub>N/Ga<sub>N</sub> HEMT for Microwave Applications", Parvesh Gangwani, Ravneet Kaur, Sujata Pandey, Subhasis Haldar, Mridula Gupta, R. S. Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [123]. "Pre-Distortion Linearity Enhancement for Sub-50nm Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET", Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta, R.S. Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [124]. "Electrical Characterization of Insulated Shallow Extension (ISE) MOSFET: A Punchthrough Stopper", Ravneet Kaur, Rishu Chaujar, Manoj Saxena, R.S. Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [125]. "An Analytical 2-Dimensional Subthreshold Model for Drain Induced Barrier Lowering Effect in Sub-Micron Ga<sub>N</sub> MESFET", Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta, RS Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [126]. "An Analytical Model for Graded Channel Asymmetric Gate Stack Surrounding Gate MOSFET (GCASYMGAS SGT)", Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, R.S Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [127]. "Analytical Modeling and Simulation of Small Geometry AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs", Sona Kumar, Anju Agrawal, Rishu Chaujar, Sneha Kabra, Mridula Gupta, R.S. Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [128]. "Impact of Innovative Gate Insulator Geometries and Their Thickness Scaling on the Device Performance of AlGa<sub>N</sub>/Ga<sub>N</sub> MISHFET for Microwave Applications", Ruchika Aggarwal, Anju Agrawal, Mridula Gupta, R.S. Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [129]. "Scrutinize the gate misalignment effects in graded channel DG FD SOI n-MOSFET", Rupendra Kumar Sharma, Manoj Saxena, Mridula Gupta and R.S. Gupta, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.



- [130]. “*A TCAD study of Sub-100 nm Advance Gate Electrode Workfunction Engineered SON-MOSFET*”, R.S. Gupta, Manoj Saxena and Poonam Kasturi, 11th International Symposium on Microwave and Optical Technology (ISMOT-2007), Villa Mondragone, Monte Porzio Catone, Italy, 17-21 December 2007.
- [131]. “*Two-Dimensional Analytical Sub-Threshold Modeling and Simulation of Gate Material Engineered HEMT For Enhanced Carrier Transport Efficiency*”, Sona P. Kumar, Anju Agrawal, Rishu Chaujar, Mridula Gupta and R.S.Gupta, International Semiconductor Device Research Symposium (ISDRS-2007), Maryland, USA, 12-14 December, 2007.
- [132]. “*On-State and Switching Performance Investigation of Sub-50nm L-DUMGAC MOSFET Design for High Speed Logic Applications*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S.Gupta, International Semiconductor Device Research Symposium (ISDRS-2007), Maryland, USA, 12-14 December, 2007.
- [133]. “*Impact of Laterally Asymmetric Channel and Gate Stack Architecture on Device Performance of Surrounding Gate MOSFET: A Simulation Study*”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, International Semiconductor Device Research Symposium (ISDRS-2007), Maryland, USA, 12-14 December, 2007.
- [134]. “*2-Dimensional simulation and characterization of deep-submicron AlGaIn/GaN HEMTs for high frequency applications*”, Parvesh, Ravneet Kaur, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R.S. Gupta, International Semiconductor Device Research Symposium (ISDRS-2007), Maryland, USA, 12-14 December, 2007.
- [135]. “*Gate Dielectric Engineering of Sub Quarter Micron AlGaIn/GaN Metal Insulator Semiconductor Heterostructure Field Effect Transistor (MISHFET) for High Gain Characteristics*”, Ruchika Aggarwal, Anju Agarwal, Mridula Gupta, International Semiconductor Device Research Symposium (ISDRS-2007), Maryland, USA, 12-14 December, 2007.
- [136]. “*Dual Material Gate (DMG) SOI-MOSFET with Dielectric Pockets: Innovative Sub-50 nm design for improved switching performance*”, Ravneet Kaur, Rishu Chaujar, Manoj Saxena, and R. S. Gupta, Indo-Australian Symposium on Multifunctional Nanomaterials, Nanostructures and Applications (MNNA 2007), pp.109, December 19–21, 2007, New Delhi, India.
- [137]. “*Two-Dimensional Analytical Modeling and Simulation of Rectangular Gate Recessed Channel (RG-RC) Nanoscale MOSFET in Sub-50nm Regime*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, Indo-Australian Symposium on Multifunctional Nanomaterials, Nanostructures and Applications (MNNA 2007), pp.110, December 19–21, 2007, New Delhi, India
- [138]. “*TCAD Investigation of a Novel MOSFET Architecture of DMG ISE SON MOSFET for ULSI Era*” Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.

- [139]. “*Analytical Analysis of Subthreshold Performance of Sub-100nm Advanced MOSFET Structures-An Iterative Approach*” Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [140]. “*Modeling and 2-D Simulation of Nanoscale SON MOSFET*” Poonam Kasturi, Manoj Saxena, Mridula Gupta and R.S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India
- [141]. “*Performance Advantage of Air as Buried Dielectric in Sub-100 nm Silicon-on-Nothing (SON) MOSFET with Gate Stack Architecture*”, Poonam Kasturi, Manoj Saxena, Mridula Gupta and R.S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [142]. “*Sub-Threshold Drain Current Performance Assessment of MLGEWE-RC MOSFET for CMOS Technology*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [143]. “*RF Performance Assessment of L-DUMGAC MOSFET for Future CMOS Technology in GigaHertz Regime*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [144]. “*Impact of GME Design on Nanometer HEMT Capacitances and its Influence on Device RF Performance*”, Sona P. Kumar, Anju Agrawal, Rishu Chaujar, Mridula Gupta and R. S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [145]. “*Nanoscale HEMT with GME Design for High Performance Analog Applications*”, Sona P. Kumar, Anju Agrawal, Rishu Chaujar, Mridula Gupta and R. S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [146]. “*Modeling of nitride based Hetrojunction Transistors for RF Applications*”, Parvesh, Ravneet Kaur, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R S Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [147]. “*Temperature Dependent Analytical Model of AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT*”, Parvesh, Ravneet Kaur, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R S Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.
- [148]. “*Impact of Gate Stack Architecture on Device Characteristics of Surrounding Gate MOSFETs*”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S.Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.

[149]. “*Modeling and Simulation of Graded Channel Asymmetric Gate Stack (GCASYMGAS) Surrounding Gate MOSFET*”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R. S. Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.

[150]. “*High Temperature Modeling of AlGaIn/GaN MISHFET and Its Relative Comparison with Conventional HFET for Microwave, Power and Switching Applications*”, Ruchika Aggarwal, Anju Agrawal, Mridula Gupta and R.S.Gupta, Mini-Colloquia on Compact Modeling of Advance MOSFET Structures and Mixed Mode Applications, January 5-6, 2008, New Delhi, India.

[151]. “*Linearity Performance Enhancement of DMG AlGaIn/GaN High Electron Mobility Transistor*”, Sona P. Kumar, Anju Agarwal, Rishu Chaujar, Mridula Gupta and R.S. Gupta, 11th International Conference on Modeling and Simulation of Microsystems (MSM-2008), June 1-5, 2008, Boston, Massachusetts, USA, 2008.

[152]. “*Compact Analytical Threshold Voltage Model for Nanoscale Multi-Layered-Gate Electrode Workfunction Engineered Recessed Channel (MLGEWE-RC) MOSFET*”, R.Chaujar, R.Kaur, M.Saxena, M.Gupta and R. S. Gupta, 2008 Workshop on Compact Modeling (WCM-2008), June 1-5, 2008, Boston, Massachusetts, U.S.A 2008.

[153]. “*Assessment of L-DUMGAC MOSFET for High Performance RF Applications with Intrinsic Delay and Stability as Design Tools*”, R.Chaujar, R.Kaur, M.Saxena, M.Gupta and R. S. Gupta, 11th International Conference on Modeling and Simulation of Microsystems (MSM-2008), June 1-5, 2008, Boston, Massachusetts, U.S.A., 2008.

[154]. “*Pre-Distortion Assessment of Workfunction Engineered Multi-Layer Dielectric Design of DMG ISE SON MOSFET*”, R.Kaur, R.Chaujar, M.Saxena, M.Gupta and R. S. Gupta, 11th International Conference on Modeling and Simulation of Microsystems (MSM-2008), June 1-5, 2008, Boston, Massachusetts, U.S.A., 2008.

[155]. “*An Iterative Approach to Characterize Various Advanced Non-Uniformly Doped Channel Profiles*”, R.Kaur, R.Chaujar, M.Saxena, M.Gupta and R. S. Gupta, Communicated to 2008 Workshop on Compact Modeling (WCM-2008), June 1-5, 2008, Boston, Massachusetts, U.S.A., 2008.

[156]. “*Linearity Performance Enhancement of DMG AlGaIn/GaN High Electron Mobility Transistor*”, S.P.Kumar, A.Agrawal, R.Chaujar, M.Gupta and R. S. Gupta, Communicated to 11th International Conference on Modeling and Simulation of Microsystems (MSM-2008), June 1-5, 2008, Boston, Massachusetts, U.S.A., 2008.

[157]. “*Nanoscale Analytical Modeling and TCAD Simulation SDPI MOSFET*”, Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, IEEE International Nanoelectronics Conference (INEC-2008), March 24-27, 2008, Shanghai, China, 2008.

[158]. “*TCAD Investigation of Hot Carrier Reliability Issues Associated with GEWE-RC MOSFET*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, IEEE International Nanoelectronics Conference (INEC-2008), March 24-27, 2008, Shanghai, China, 2008.

[159]. “*Impact of Non-Uniformly Doped and MultiLayered Asymmetric Gate Stack Design on Device Characteristics of Surrounding Gate MOSFETs*”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R. S. Gupta, 2008 NSTI Nanotechnology Conference and Trade Show, Boston, Massachusetts, U.S.A., June 1-5, 2008.

[160]. “*A Comparative Analysis Using Modeling and Simulation to Study the Impact of Multilayered Gate Dielectric (MGD) Design on Device Performance of Surrounding Gate MOSFET*”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, XXIX General Assembly of the International Union of Radio Science, (Union Radio Scientifique Internationale – URSI), Illinois, USA, August 07-16, 2008.

[161]. *Impact of Multi-layered Gate Design on Hot Carrier Reliability of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, XXIX General Assembly of the International Union of Radio Science, (Union Radio Scientifique Internationale – URSI), Illinois, USA, August 07-16, 2008.

[162]. “*Investigation the Linearity Performance of DMG AlGaN/GaN HEMT for Improved RF Applications*”, Sona P. Kumar, Anju Agrawal, Rishu Chaujar, Mridula Gupta and R.S. Gupta, XXIX General Assembly of the International Union of Radio Science, (Union Radio Scientifique Internationale – URSI), Illinois, USA, August 07-16, 2008.

[163]. “*RF Performance Investigation of DMG AlGaN/GaN High Electron Mobility Transistor*”, Sona P.Kumar, Anju Agrawal, Rishu Chaujar, Mridula Gupta and R. S. Gupta, Interantional Conference On Recent Advancements in Microwave Theory and Applications (Microwave-2008), November 21-24, 2008, Jaipur, India.

[164]. “*Optimization of the Gate Misalignment Effects in Graded Channel DG FD SOI n-MOSFET with High Gate Dielectrics*”, Rupendra Kumar Sharma, Mridula Gupta and R. S. Gupta, Interantional Conference On Recent Advancements in Microwave Theory and Applications (Microwave-2008), November 21-24, 2008, Jaipur, India.

[165]. “*Impact of Gate Stack Configuration into the RF/Analog Performance of ISE MOSFET*”, Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, Interantional Conference On Recent Advancements in Microwave Theory and Applications (Microwave-2008), November 21-24, 2008, Jaipur, India.

[166]. “*GEWE-RC MOSFET: A Solution to CMOS Technology for RFIC Design Based on the concept of Intercept Point*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, International Conference on Recent Advancesments in Microwave Theory and Applications (Microwave-2008), Jaipur, India November 21-24, 2008.

[167]. “*Investigation of temperature dependent microwave performance of AlGaN/GaN MISHFETs for high power wireless applications*”, Ruchika Aggarwal, Anju Agrawal, Mridula Gupta and R.S. Gupta, International Conference on Recent Advancesments in Microwave Theory and Applications (Microwave-2008), Jaipur, India November 21-24, 2008.

- [168]. “Comparative subthreshold analysis for channel depth variation on sub-100 nm double-gate and single-gate HEMT”, Servin Rathi, Ritesh Gupta, Mridula Gupta and R.S. Gupta, International Conference on Recent Advancements in Microwave Theory and Applications (Microwave-2008), Jaipur, India November 21-24, 2008.
- [169]. “Exploring the effect of negative junction depth on electrical behaviour of sub-50nm GME-TRC MOSFET: A simulation study”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S. Gupta, International Conference on Recent Advancements in Microwave Theory and Applications (Microwave-2008), Jaipur, India Nov. 21-24, 2008.
- [170]. “Two Dimensional Analytical Modeling of Multi-Layered Dielectric G4-MOSFET - A Novel Design”, (Invited Talk) R.S. Gupta, Namita Sharma, Jyoti Bansal, Rishu Chaujar and Mridula Gupta, International Conference on Recent Advancements in Microwave Theory and Applications (Microwave-2008), Jaipur, India November 21-24, 2008.
- [171]. “Characterization asymmetric multilayered gate dielectric (AMGAD) surrounding gate MOSFET : A new structural concept for enhanced device performance”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar, and R. S. Gupta, International Conference on Recent Advancements in Microwave Theory and Applications (Microwave-2008), Jaipur, India November 21-24, 2008.
- [172]. “Analytical approach for high temperature analysis of AlGaN/GaN HEMT”, Parvesh, Ravneet Kaur, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R S Gupta, International Conference on Recent Advancements in Microwave Theory and Applications (Microwave-2008), Jaipur, India November 21-24, 2008.
- [173]. “DMG AlGaN/GaN HEMT: A solution to RF and wireless applications for reduced distortion performance”, S. P. Kumar, A. Aggarwal, R. Chaujar, M. Gupta and R.S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.
- [174]. “TCAD Performance Investigation of a Novel MOSFET Architecture of Dual Material Gate Insulated Shallow Extension Silicon On Nothing (DMG ISE SON) MOSFET for ULSI era”, R. Kaur, R. Chaujar, M. Saxena, R.S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.
- [175]. “Capacitance modeling of 120nm AlGaN/GaN HEMT for microwave and high speed circuit applications”, P. Gangwani, R. Kaur, S. Haldar, M. Gupta and R.S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.
- [176]. “AlGaN/GaN MISHFET: A Novel Alternative to Power HFETs for High Temperature Microwave Digital and Switching Applications”, R. Aggarwal, A. Aggarwal, M. Gupta and R.S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.
- [177]. “Impact of Laterally Asymmetric Channel and Gate Stack Design on Device Performance of Surrounding Gate MOSFETs : A Modeling and Simulation Study”, H. Kaur, S. Kabra, S. Haldar and R.S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.

[178]. “*Gate material engineered-trapezoidal recessed channel MOSFET (GME-TRC) for ultra large scale integration (ULSI)*”, P. Malik, S.P. Kumar, R. Chaujar, M. Gupta and R.S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.

[179]. “*GEWE-RC MOSFET: High Performance RF Solution to CMOS Technology*”, R. Chaujar, R. Kaur, M. Saxena, M. Gupta and R.S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.

[180]. “*High Tolerance to Gate Misalignment in Graded Channel Double Gate SOI n-MOSFETs: Small Signal parameter Analysis*”, Rupendra Kumar Sharma, Ritesh Gupta, Mridula Gupta and R. S. Gupta, 2008 Asia-Pacific Microwave Conference, Hong Kong and Macau, Dec. 16-19, 2008 and Dec. 19-20, 2008.

[181]. “*A Simulated Study of Gate Misalignment Effects on the Dynamic Performance of Nanoscale Double Gate and Dual Material Double Gate SOI n-MOSFET*” Rupendra Sharma, Mridula Gupta, R. S. Gupta, 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.

[182]. “*Sub 100nm Double Gate MOSFETs: A Study of Technological Defects and Carrier Quantization Effects*” Amit Sehgal, Ritesh Gupta, Mridula Gupta, R S Gupta, 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.

[183]. “*Two-dimensional Analytical Model for Trapezoidal Recessed Channel (TRC) MOSFET using Gate Material Engineering*”, Priyanka Malik, Rishu Chaujar, Mridula Gupta, R S Gupta, 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.

[184]. “*High Temperature Modeling of AlGaIn/GaN HEMT For Microwave Power and Switching Applications*” Parvesh Gangwani, Subhasis Haldar, Mridula Gupta, R.S. Gupta 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.

[185]. “*Microwave Performance Evaluation of DMG AlGaIn/GaN HEMT: A Simulation Study*” Sona P. Kumar, A. Agrawal, Mridula Gupta, R.S. Gupta, 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.

[186]. “*Analytical Drain Current Evaluation Technique for Various Non-Uniformly Doped MOS Device Architectures*” Ravneet Kaur, Manoj Saxena, R.S. Gupta, 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.

[187]. “*Evaluation of Multi-Layered Gate Design on GEWE-RC MOSFET for Wireless Applications in terms of Linearity-Distortion Issues*”, Rishu Chaujar, Manoj Saxena, Mridula Gupta, R.S. Gupta, 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.

- [188]. “Comparative Performance Evaluation of Novel AlGa<sub>N</sub>/Ga<sub>N</sub> MISHFET with Conventional HFET for Improved Linearity Characteristics”, Ruchika Aggarwal, Anju Agrawal, Mridula Gupta, R. S. Gupta, 12th International Symposium on Microwave and Optical Technology (ISMOT-2009) will be held at Hotel Ashok, New Delhi, India from 16 - 19, December 2009.
- [189]. “Analytical modeling of channel noise for gate material engineered surrounded/cylindrical gate (SGT/CGT) MOSFET”, Pujarini Ghosh, Rishu Chaujar, Subhasis Halder, Mridula Gupta and R.S. Gupta, (ICMED -2010), Rome, Italy, April 28 – 30, 2010.
- [190]. “Two-dimensional analytical drain current model for Multilayered-Gate Material Engineered Trapezoidal Recessed Channel (MLGME-TRC) MOSFET: a novel design”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S.Gupta, ICMED 2010: "International Conference on Microelectronics and Electron Devices", Rome, Italy, April 28-30, 2010.
- [191]. “Microwave and RF Applications of Gate Material Engineered Trapezoidal Recessed Channel (GME-TRC) MOSFET”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S.Gupta, Nanotech conference and Expo 2010, Anaheim, CA, United state of America, June, 2010.
- [192]. “Linearity Performance Assessment of Nanoscale Gate Material Engineered Trapezoidal Recessed Channel (GME-TRC) MOSFET for RFIC design and Wireless application”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S.Gupta, Nanotech conference and Expo 2010, Anaheim, CA, United state of America, June, 2010.
- [193]. “Evaluation of Multi-Layered Gate Design on GME-TRC MOSFET for Wireless Applications”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S. Gupta, IEEE International Conference on Semiconductor Electronics (ICSE2010), Holiday Inn Melaka Hotel, Melaka, Malaysia, June 28-30, 2010.
- [194]. “Analytical channel carrier noise temperature model for gate material engineered SGT/CGT MOSFET”, Pujarini Ghosh, Rishu Chaujar, Subhasis Halder, R.S. Gupta and Mridula Gupta. International Conference on “NANO Technology - Materials & Composites for Frontier Applications (NANOCON-2010), Pune, India, Oct 14-15, 2010
- [195]. “Impact of Doping concentration and Donor-layer thickness on the de characterization of symmetric double-gate and single-gate InAlAs/InGaAs/InP HEMT for nanometer gate dimension-A comparision”, Monika Bhattacharya, Jyotika Jogi, Mridula Gupta, R.S Gupta. IEEE (TENCON-2010), Fukuoka, Fukuoka International Congress Center, Japan, Nov 21-24, 2010.
- [196]. “A Unified Two Dimensional Analytical Model Of Optically Controlled Silicon On Insulator MESFET (Opsoi ) For Advanced Channel Materials”, Rajni Gautam, Manoj Saxena, R.S. Gupta and Mridula Gupta. 10<sup>th</sup> International Conference on Fibre Optics and Photonics (PHOTONICS-2010), Indian Institute of Technology Guwahati, Assam, India Dec 11-15, 2010.
- [197]. “The analytical drain current model for Dual Metal Gate Cylindrical Gate MOSFET”, Pujarini Ghosh, Subhasis Halder, R.S. Gupta and Mridula Gupta. International Conference on Microwaves, Antenna, Propagation & Remote Sensing. (ICMARS-2010),Jodhpur, Rajasthan, India. Dec 14-17, 2010.

- [198]. “*An analytical study of enhanced microwave performance of symmetric double-gate InAlAs/InGaAs/InP HEMT over single-gate InAlAs/InGaAs/InP HEMT for nanometer gate dimension*” Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta. International Conference on Microwaves, Antenna, Propagation & Remote Sensing. (ICMARS-2010), Jodhpur, Rajasthan, India. Dec 14-17, 2010.
- [199]. “*Simulation Study of Gate Stacked Insulated Shallow Extension Silicon On Nothing ISE-SON MOSFET for RFICs design*”, Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta. IEEE Student’s Technology Symposium, Indian Institute of Technology Kharagpur, India. Jan 14-16, 2011
- [200]. “*Modeling and Simulation of Multi layer gate dielectric Double Gate Tunnel Field Effect Transistor (DGTFT)*”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta. IEEE Student’s Technology Symposium, Indian Institute of Technology Kharagpur, India. Jan 14-16, 2011.
- [201]. “*Analysis and Simulation of Si/GaAs/GaN MESFET to study the Impact of Localised Charges on Device Performance*”, Rajni Gautam, Manoj Saxena, R. S. Gupta and Mridula Gupta. IEEE Student’s Technology Symposium, Indian Institute of Technology Kharagpur, India. Jan 14-16, 2011.
- [202]. “*Analytical Modeling of Intrinsic Y-parameters to study the enhanced microwave performance of symmetric tied-gate InAlAs/InGaAs/InP DG-HEM*”, Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta. International Conference on Signal, Systems and Automation (ICSSA-2011), G.H Patel College of Engineering, Anand, Gujrat, India. Jan 24-25, 2011.
- [203]. “*RF performance of Gate Material Engineered Surrounded/Cylindrical MOSFETs for High-speed applications*”, Pujarini Ghosh, Subhasis Haldar, R.S. Gupta and Mridula Gupta. International Conference on Microelectronics and Electron Devices (ICMED-2011), Penang Malaysia, Feb 22-24, 2011.
- [204]. “*Estimation of performance degradation of the nanoscale Cylindrical Surrounded gate MOSFET due to hot carrier induced localised charges*”, Rajni Gautam, Manoj Saxena, R. S. Gupta and Mridula Gupta. International Conference on Latest Trends in Nanoscience and Nanotechnology (ICNSNT-2011), Gulbarga, Khaja BandaNawaz College of Engineering, Karnataka, India. March 28-29, 2011.
- [205]. “*Impact of a Low Bandgap Material on the Linearity of a DG-TFET: A Comparative Study*”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta. International Conference on Latest Trends in Nanoscience and Nanotechnology (ICNSNT-2011), Gulbarga, Khaja BandaNawaz College of Engineering, Karnataka, India. March 28-29, 2011.
- [206]. “*Nanoscale Double Gate Silicon On Nothing (DGSON) MOSFET: Promising Device Design for Wide Range of Operating Temperatures*”, Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta, International Conference on Latest Trends in Nanoscience and Nanotechnology (ICNSNT-2011), Gulbarga, Khaja BandaNawaz College of Engineering, Karnataka, India. March 28-29, 2011.



- [207]. “*High Sensitivity Photodetector Using Si/Ge/GaAs Metal Semiconductor Field Effect Transistor (MESFET)*”, Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta. A Conference on Light (OPTICS-11), Calicut, Kerala, India. May 23-25, 2011.
- [208]. “*A Comprehensive Analytical Approach for drain-noise source and gate-noise source modeling of InAlAs/InGaAs DG-HEMT*”, Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta, International Conference on microwave and Optical technology (ISMOT-2011,) Prague, Czech Republic, EU. June 20-23, 2011.
- [209]. “*Analytical investigating of the enhanced dynamic performance of  $In_{0.52}Al_{0.48}As-In_{0.53}Ga_{0.47}As$  Separate DG-HEMT for nanometer gate dimension*”, Parveen, Mridula Gupta, R.S. Gupta and Jyotika Jogi. International Conference on microwave and Optical technology (ISMOT-2011), Prague, Czech Republic, EU. June 20-23, 2011.
- [210]. “*Analytical Capacitance Model of Dual Metal Surrounded/Cylindrical Gate MOSFETs*”, Pujarini Ghosh, Subhasis Halder, R.S. Gupta and Mridula Gupta. International Conference on microwave and Optical technology (ISMOT-2011), Prague, Czech Republic, EU. June 20-23, 2011.
- [211]. “*RF Performance of Gate Material Engineered Trapezoidal Recessed Channel (GME-TRC) MOSFET for Microwave design*”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S. Gupta, International Conference on microwave and Optical technology (ISMOT-2011), Prague, Czech Republic, EU. June 20-23, 2011.
- [212]. “*Impact of Localized Charges on RF and Microwave Performance of Nanoscale Surrounding Cylindrical Gate MOSFET*”, Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, International Conference on microwave and Optical technology (ISMOT-2011), Prague, Czech Republic, EU. June 20-23, 2011.
- [213]. “*RF Performance Analysis of Double Gate Tunneling Field Effect Transistor (DG-TFET)*”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta. International Conference on microwave and Optical technology (ISMOT-2011), Prague, Czech Republic, EU. June 20-23, 2011.
- [214]. “*Comparative Study of Dielectric Pocket (DP) MOSFET Incorporating Buried Oxide Layer (BOX) with DP MOSFET for RF Applications*”, Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta. International Conference on microwave and Optical technology (ISMOT-2011), Prague, Czech Republic, EU. June 20-23, 2011.
- [215]. “*Effect of Gate Length Scaling on the Linearity Characteristics of AlGaIn/GaN MISHFET: An Analytical study*” Ruchika Aggarwal, Anju Agrawal, Mridula Gupta, R.S. Gupta. International Conference on microwave and Optical technology (ISMOT-2011), Prague, Czech Republic, EU. June 20-23, 2011.
- [216]. “*SiGe Metal Semiconductor Field Effect Transistor (MESFET) Photodetector Having Tailorable Photoresponse Using Bandgap Engineering*” Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta. International conference on materials for advanced technologies (ICMAT-2011) Suntec, Singapore, June- July 26-1, 2011.

- [217]. “Immunity Against Temperature Variability and Bias Point Invariability in Double Gate Tunnel Field Effect Transistor”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta International conference on materials for advanced technologies (ICMAT-2011) Suntec, Singapore , June- July 26-1, 2011.
- [218]. “*Simulation Study of Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET for High Temperature Applications*”, Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta. International conference on materials for advanced technologies (ICMAT-2011) Suntec, Singapore , June- July 26-1, 2011.
- [219]. “*A Wide Temperature Range ( 50- 500K ) Analysis For Nanoscale Surrounding Cylindrical Gate MOSFET With Localised Charges*”, Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, VLSI Design And Test Symposium (VDAT), Pune, Maharashtra, India July 7-9, 2011.
- [220]. “*Analog Performance of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET: Simulation study*”, Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta. VLSI Design And Test Symposium (VDAT), Pune, Maharashtra, India July 7-9, 2011.
- [221]. “*Investigation of Linearity Performance of a Double Gate Band to Band Tunnel Field Effect Transistor*”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta. VLSI Design And Test Symposium (VDAT), Pune, Maharashtra, India July 7-9, 2011.
- [222]. “*Channel Material Engineered Nanoscale Cylindrical Surrounding Gate MOSFET With Interface Fixed Charges*”, Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, The Second International workshop on VLSI (VLSI 2011), The Park Hotels, Chennai, India, July 15 - 17, 2011
- [223]. “*Effect of Temperature and Gate Stack on the Linearity and Analog Performance of Double Gate Tunnel FET*”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta. The Second International workshop on VLSI (VLSI 2011), The Park Hotels, Chennai, India, July 15 - 17, 2011
- [224]. “*An Analytical study of the impact of gate-bias on the scattering parameters of a symmetric tied-gate InAlAs/InGaAs DG-HEMT*”, Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta, International Symposium on Models and Modeling Methodologies in Science and Engineering (IS-MMMSe 2011) Orlando, Florida, USA, July 19 -22, 2011.
- [225]. “*A Comprehensive Analytical approach for the evaluation of the P,R and C noise coefficients of InAlAs/InGaAs DG-HEMT*”, Monika Bhattacharya, Jyotika Jogi, R.S. Gupta and Mridula Gupta, IEEE TENCON, Bali, Indonesia, Nov 21-24, 2011.
- [226]. “*A Small Signal Intrinsic Equivalent Circuit Model for Cylindrical/Surrounded Gate MOSFET for Microwave Frequency Applications*”, Pujarini Ghosh, Subhasis Haldar, R.S.Gupta. and Mridula Gupta, Asia Pacific Microwave Conference (APMC 2011). Melbourne, Australia, December 5-8, 2011.
- [227]. “*Linearity performance and Intermodulation distortion Analysis of Gate Material Engineered Cylindrical Gate MOSFET*”, Pujarini Ghosh, Subhasis Haldar, R.S.Gupta. and Mridula Gupta, International workshop on physics of semiconductor devices (IWPSD 2011) IIT Kanpur, India December 19-22, 2011.

- [228]. “*A comprehensive charge control based analysis of the effect of Donor-layer doping and donor-layer thickness on the P, R and C noise coefficients of a symmetric tied-gate InAlAs/InGaAs DG-HEMT*”, Monika Bhattacharya, Jyotika Jogi, R.S. Gupta and Mridula Gupta. International workshop on physics of semiconductor devices (IWPSD 2011) IIT Kanpur, India December 19-22, 2011.
- [229]. “*An Analytical Modeling Approach for a Gate All Around (GAA) Tunnel Field Effect Transistor (TFET)*”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta, International workshop on physics of semiconductor devices (IWPSD 2011) IIT Kanpur, India December 19-22, 2011.
- [230]. “*Digital Circuit Analysis of Insulated Shallow Extension Silicon On Void (ISESOV) FET for Low Voltage Applications*”, Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta, International workshop on physics of semiconductor devices (IWPSD 2011) IIT Kanpur, India December 19-22, 2011.
- [231]. “*Influence of Localised charges on the temperature sensitivity of Si nanowire MOSFET*” Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, International workshop on physics of semiconductor devices (IWPSD 2011) IIT Kanpur, India December 19-22, 2011.
- [232]. “*Analytical Modeling and Simulation for Dual metal Symmetrical Gate Stack (DMGAS) Cylindrical/Surrounded Gate MOSFET*”, Pujarini Ghosh, Subhasis Haldar, R.S.Gupta. and Mridula Gupta , International Semiconductor Device Research Symposium (ISDRS-2011) College Park, Maryland, December 7-9, 2011.
- [233]. “*Modeling and Simulation of Dielectric Pocket Double Gate (DP-DG) MOSFET for Low Voltage Low Power Analog Applications*”, Vandana Kumari, Manoj Saxena, R. S. Gupta and Mridula Gupta, International Semiconductor Device Research Symposium (ISDRS-2011) College Park, Maryland, December 7-9, 2011.
- [234]. “*Analytical Modeling of the Impact of Drain Voltage on P, R and C Noise Coefficients for a Symmetric Tied-gate InAlAs/InGaAs DG-HEMT*” Monika Bhattacharya, Jyotika Jogi, R.S. Gupta and Mridula Gupta, International Semiconductor Device Research Symposium (ISDRS-2011) College Park, Maryland, December 7-9, 2011.
- [235]. “*Investigation of RF/Microwave Performance Degradation for Cylindrical Nanowire MOSFET Due to Interface (Localised) Charges*” Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, International Semiconductor Device Research Symposium (ISDRS-2011) College Park, Maryland, December 7-9, 2011.
- [236]. “*Analytical Model of a Tunnel FET Based Biosensor for Label Free Detection*” Rakhi Narang, K. V. Sasidhar Reddy, Manoj Saxena, R.S. Gupta and Mridula Gupta , International Semiconductor Device Research Symposium (ISDRS-2011) College Park, Maryland, December 7-9, 2011.
- [237]. “*Quantum Modeling of Electron Confinement in Double Triangular Quantum Well Formed in Nanoscale Symmetric Double-Gate InAlAs/InGaAs/InP HEMT*” Jyotika Jogi, Neha Verma, Mridula Gupta and R.S. Gupta and. International Semiconductor Device Research Symposium (ISDRS-2011) College Park, Maryland, December 7-9, 2011.

- [238]. “Analytical modeling of Enhanced Performance of Separate Gate  $In_{0.52}Al_{0.48}As$   $In_{0.53}Ga_{0.47}As$  DG-HEMT for Nanometer Gate Dimension, Parveen, Mridula Gupta, R.S. Gupta and Jyotika Jogi. International Conference on Microwaves, Antenna, Propagation & Remote Sensing” (ICMARS-2010), Jodhpur, Rajasthan, India December 7-10, 2011.
- [239]. “Dynamic Performance Comparison of  $p-i-n$  and  $p-n-p-n$  Tunnel Field Effect Transistor and Impact of Gate Drain underlap” Rakhi Narang, Manoj Saxena, R.S. Gupta and Mridula Gupta International Conference on Nano Science and Technology (ICONSAT 2012), Hyderabad. India, January 20-23, 2012.
- [240]. “Temperature dependent RF/microwave characteristics of nanowire surrounding gate mosfet with localized charges” Rajni Gautam, Manoj Saxena, R.S. Gupta and Mridula Gupta International Conference on Nano Science and Technology (ICONSAT 2012), Hyderabad. India, January 20-23, 2012.
- [241]. “Nano-scale Empty Space in Double Gate (ESDG) MOSFET for High Performance Digital Applications: A Theoretical Study ” Vandana Kumari, Manoj Saxena, R.S. Gupta and Mridula Gupta International Conference on Nano Science and Technology (ICONSAT 2012), Hyderabad. India, January 20-23, 2012.
- [242]. “Asymmetric Gate Oxide Tunnel Field Effect Transistor for Improved Circuit Performance” Rakhi Narang, Manoj Saxena, R. S. Gupta, and Mridula Gupta, IEEE International Conference on Devices, Circuits and Systems (ICDCS 2012), Karunya University, Coimbatore, Tamil Nadu, India, March 15-16, 2012.
- [243]. “Impact of Localised Charges Present in the Interfacial Layer of the Schottky Contact in SOI MESFET”, Rajni Gautam, Manoj Saxena, R.S.Gupta, and Mridula Gupta, IEEE International Conference on Devices, Circuits and Systems (ICDCS 2012), Karunya University, Coimbatore, Tamil Nadu, India, March 15-16, 2012.
- [244]. “Laterally-Asymmetric- Channel-Insulated-Shallow Extension-Silicon-On-Nothing LAC-ISE-SON MOSFET for Improved Reliability and Digital Circuit Simulation”, Vandana Kumari, Manoj Saxena, R.S.Gupta, and Mridula Gupta, IEEE International Conference on Devices, Circuits and Systems (ICDCS 2012), Karunya University, Coimbatore, Tamil Nadu, India, March 15-16, 2012.
- [245]. “Tunnel FET as a Biomolecule Sensor” Mridula Gupta (Invited Lecture 15), International conference on VLSI, MEMS & NEMS. (VMN 2012), Amity School of Engineering & Technology, Amity University, Uttar Pradesh.
- [246]. “Physics based Analytical Model for a Pocket Doped  $p-n-p-n$  Tunnel Field Effect Transistor”, Rakhi Narang, Manoj Saxena, R. S. Gupta, and Mridula Gupta. Tech-Connect World 2012 , Santa Clara, CA, USA., June 18-21, 2012.
- [247]. “Analytical Drain Current Model For Damaged Gate All Around (GAA) MOSFET Including Quantum and Velocity Overshoot Effects”, Rajni Gautam, Manoj Saxena, R. S. Gupta and Mridula Gupta. Tech-Connect World 2012 Tech-Connect World 2012 , Santa Clara, CA, USA., June 18-21, 2012.

- [248]. “*A comprehensive charge control based analysis of the effect of Donor-layer doping and donor-layer thickness on the P, R and C noise coefficients of a symmetric tied-gate InAlAs/InGaAs DG-HEMT*” Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta, (Accepted for Publication in SPIE Digital Library)
- [249]. “*An Analytical Modeling Approach for a Gate All Around (GAA) Tunnel Field Effect Transistor (TFET)*” Rakhi Narang, Manoj Saxena, R. S. Gupta, and Mridula Gupta (Accepted for Publication in SPIE Digital Library)
- [250]. “*Digital circuit analysis of Insulated Shallow Extension Silicon On Void (ISESOV) FET for low voltage application*”. Vandana Kumari, Manoj Saxena, R.S. Gupta and Mridula Gupta (Accepted for Publication in SPIE Digital Library)
- [251]. “*Temperature and Channel Indium Composition Sensitivity Analysis of the Small-Signal Equivalent Circuit Parameters of SG- and DG- InAlAs/InGaAs HEMT*”, Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta, NANOCON-2012, 18-19 Oct 2012, Pune, Maharashtra.
- [252]. “*Gate All Around Mosfet With Catalytic Metal Gate For Gas Sensing Applications*”, Rajni Gautam, Manoj Saxena, R.S.Gupta, and Mridula Gupta NANOCON 2012, 18-19<sup>th</sup> Oct, 2012, Pune, Maharashtra.
- [253]. “*Comparative study of Silicon on Nothing and III-V On Nothing architecture for High speed and Low Power analog and RF/Digital Applications*” Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta, NANOCON 2012, 18-19<sup>th</sup> Oct, 2012, Pune, Maharashtra.
- [254]. “*Impact of temperature variations on the device and circuit performance of Tunnel FET - A Simulation Study*” Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta, NANOCON 2012, 18-19<sup>th</sup> Oct, 2012, Pune, Maharashtra.
- [255]. “*Analytical Model for a Dielectric Modulated Double Gate FET (DM-DG-FET) Biosensor*”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta, ICEE 2012, IIT Bombay 15-17 December, 2012
- [256]. “*Temperature Dependent Model for Dielectric Pocket Double Gate (DPDG) MOSFET: A Novel Device Architecture*” Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ICEE 2012, IIT Bombay 15-17 December, 2012
- [257]. “*RF performance of Dual Metal Cylindrical/Surrounded Gate MOSFET for High Switching Speed Applications*”, Pujarini Ghosh, Subhasis Haldar, R.S Gupta and Mridula Gupta. ICEE 2012, IIT Bombay 15-17 December, 2012.
- [258]. “*Impact of Noise Temperature Constant and Diffusion Coefficient on the Minimum Noise Figure and Minimum Noise Temperature of InAlAs/InGaAs DG-HEMT*”, Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta, ICEE 2012, IIT Bombay 15-17 December, 2012.
- [259]. “*Analog /RF Performance of Gate Material Engineering Cylindrical/ Surrounding Gate (CGT/SGT) MOSFETs*”, Yogesh Pratap, Jay hind Kumar Verma, Subhasis Haldar, R.S Gupta and Mridula Gupta, ICMARS-2012 Jodhpur 11-15 December 2012.
- [260]. “*Linearity Analysis of GME-TRC MOSFET Using SiO<sub>2</sub> as a gate Insulator at High Temperature*”, Priyanka Malik, R.S. Gupta and Mridula Gupta, ICAMR-2013, 19-20 January 2013.
- [261]. “*Linearity Performance Investigation of high-k Spacer based Junctionless Nanowire Transistor (JLNWT) for RFIC Design*,” Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, International Semiconductor Device Research Symposium (ISDRS), 11th-13th December-2013 USA.

- [262]. “*Hot Carrier Reliability Issues of Junctionless Transistor due to Interface Trap Charges for Analog /RF Applications*,” Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, International Workshop on Physics of Semiconductor Device (IWPSD), 10th-13th December-2013 Noida, India.
- [263]. “*Analytical Capacitance Modeling and Simulation of Dual material- Graded channel - Gate stack Cylindrical/Surrounding (DMGCGS CGT/SGT) MOSFET*,” J.H. K Verma, Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, International Semiconductor Device Research Symposium (ISDRS), 11th-13th December-2013, Maryland USA.
- [264]. “*Analytical Effect of ITC on the Characteristics of Junctionless Nanowire Transistor (JLNWT) for Future ULSI Applications: Semi-analytical Modeling Approach*,” Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, INDICON, 13th-15th December-2013, IIT Bombay, India.
- [265]. “*Performance Investigation of Dual Material Gate Stack Schottky-Barrier Source/Drain GAA MOSFET for Analog Applications*” Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, “ International Workshop on the Physics of Semiconductor Devices (IWPSD-2013)” , Amity University, NOIDA, India, 10<sup>th</sup>-13<sup>th</sup> December, 2013.
- [266]. “*A Comparative Assessment of Schottky-Barrier Source/Drain GAA MOSFET with Conventional and Junctionless GAA MOSFETs*”, Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta. INDICON, 13th-15th December-2013, IIT Bombay, India.
- [267]. “*A New T-Shaped Source/Drain Extension (T-SSDE) Gate Underlap GAA MOSFET with Enhanced Subthreshold Analog/RF Performance for Low Power Applications*”, Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta International Semiconductor Device Research Symposium (ISDRS), 11th-13th December-2013 USA.
- [268]. “*Scattering parameter based simulation of cylindrical double gate (CDG) MOSFET for Submillimeter-Wave Application*,” J.H.K Verma, Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, ICMARS, 11<sup>th</sup>-15<sup>th</sup> December-2013, Jodhpur. India.
- [269]. “*RF Performance Analysis and Small Signal Parameter Extraction of Cylindrical Surrounding Double Gate MOSFETs for Sub-millimeter Wave Applications*”, J.H.K Verma, Yogesh Pratap, Subhasis Haldar, Mridula Gupta and R.S. Gupta, (ICDCS), 6th-8th March-2014 Coimbatore, India.
- [270]. “*Damage Immune III-V Compound Material based Vacuum Junctionless Nanowire Transistor (VAC-JNT) for Improved Electrostatic Control and Hot Carrier Reliability*,” Yogesh Pratap, S. Haldar, R. S. Gupta and Mridula Gupta, 3rd International Conference on Nanotechnology (NANOCON04), 14<sup>th</sup>-15<sup>th</sup> October-2014, Pune, India.
- [271]. “*Nanogap Embedded Dopant Segregation Schottky Barrier Source/Drain Cylindrical Gate All Around MOSFETs with High Sensitivity: Nanosensor for Biochips*,” Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, 3rd International Conference on Nanotechnology (NANOCON04), 14<sup>th</sup>-15<sup>th</sup> October-2014, Pune, India.

- [272]. “*4H-SiC-Dopant Segregated Schottky Barrier Cylindrical Gate All Around MOSFET for High Speed and High Power Microwave Applications*”, Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, India International Conference on Power Electronics (IICPE, Kurukshetra, India), December 8-10, 2014.
- [273]. “*Silicon Carbide based DSG MOSFET for high power high speed and high frequency applications*”, India International Conference on Power Electronics (IICPE, Kurukshetra, India), December 8”, Sonam Rewari, Vandana Nath, S.S Deswal and R.S. Gupta -10, 2014.
- [274]. “*Impact of Inner Charge Control Gate on CSG MOSFET for Improved Electrostatic Integrity and RF Performance*”, Jay Hind Kumar Verma, Subhasis Haldar, R.S. Gupta and Mridula Gupta (NANOCON), 14th-15th October-2014, Pune India
- [275]. “*Material Engineering in Cylindrical Surrounding Double Gate (CSDG) MOSFETs for Enhance Electrostatic Integrity and RF Performance*” Jay Hind Kumar Verma, S. Haldar, R.S. Gupta and Mridula Gupta, (ICEE), 3rd-6th December-2014, Bangalore India.
- [276]. “*Driving current analysis for Hetero gate Dielectric - Dual Material Gate - GAA-TFET,*” Jaya Madan, R.S Gupta, Rishu Chaujar, 3rd International Conference NANOCON 014 Nanotechnology - Smart Materials, Composites, Applications and New Inventions - Date: 14th, 15th October, 2014.
- [277]. “*TCAD Analysis of Small Signal Parameters and RF Performance of Heterogeneous Gate Dielectric-Gate All Around Tunnel FET,*”Jaya Madan, R.S Gupta, Rishu Chaujar. Tech connect world innovation.
- [278]. “*Threshold voltage model of a Hetero Gate Dielectric Dual Material Gate GAA Tunnel FET,*” Jaya Madan, R.S Gupta, Rishu Chaujar. Tech Connect world innovation.
- [279]. “*Capacitive Analysis of Heterogeneous Gate Dielectric-Gate Metal Engineered–Gate All Around-Tunnel FET for RF Applications,*”Jaya Madan, R.S Gupta, Rishu Chaujar, 2<sup>nd</sup> International conference on Microelectronics, circuits and systems, Micro-2015.
- [280]. “*Drain current Analysis of Hetero Gate Dielectric-Dual Material Gate–GAA-Tunnel FET,*”Jaya Madan, R.S Gupta, Rishu Chaujar, 2<sup>nd</sup> International conference on Microelectronics, circuits and systems, Micro-2015.
- [281]. “*Impact of Heterogeneous Gate Dielectric and Gate Metal Engineering on Analog and RF Performance of GAA TFET,*”Jaya Madan, R.S. Gupta and Rishu Chaujar, 2015 International Conference on Solid State Devices and Materials (SSDM), Japan, 27-30<sup>th</sup> September, 2015.
- [282]. “*CSDG MOSFET: An advance novel architecture for CMOS technology*”, Jay Hind Kumar Verma, Yogesh Pratap, S. Haldar, R.S. Gupta and Mridula Gupta, (INDICON-2015), 17-20th December-2015, Jamia Millia Islamia, New Delhi, India.
- [283]. “*Asymmetric Vacuum gate Dielectric Schottky Barrier Gate All Around MOSFET for Ambipolarity Reduction and Improved Hot Carrier Reliability*”, Manoj Kumar, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Conference on Electron Devices and Solid-State Circuits (EDSSC’2015, Singapore), June 1-4, 2015.

- [284]. *"Impact of asymmetric gat stack on a Junctionless CSG MOSFET for enhanced Hot Carrier Reliability"*, Anirudh, Arushi, Yogesh Pratap, and R.S. Gupta, (INDICON-2015), 17-20th December-2015, Jamia Millia Islamia, New Delhi, India.
- [285]. *"AC analysis of Junctionless Double Surrounding Gate MOSFT for tera hertz applications"*, Sonam Rewari, Vandana Nath, S.S Deswal and R.S. Gupta, ICCTICT, GGSIPU, 11-13 March , Delhi, India.
- [286]. *"DMG Insulated Shallow Extension Cylindrical GAA Schottky Barrier MOSFET for Removal of Ambipolarity: A Novel approach"* Manoj Kumar, Yogesh Pratap Subhasis Haldar, Mridula Gupta and R.S. Gupta, IEEE INEC 2016, Chengdu, China, May 9 –11, 2016.
- [287]. *"Sensitivity Investigation of Gate All Around Junctionless Transistor for Hydrogen Gas Detection"*, Yogesh Pratap, Manoj Kumar, S. S. Deswal, Subhasis Haldar, R.S. Gupta and Mridula Gupta, IEEE INEC 2016, Chengdu, China, May 9 –11, 2016.



### III. Papers in National Conference

- [1]. “*Variation of current gain in p-n-p junction transistor*”, R.S. Gupta & S.S. Banerjee, I.E.R.E., Sympm. (Indian Div.) on Electronics in Industry, p.11, Sept., 1968, New Delhi.
- [2]. “*Stability of the Compound Transistor*”, R.S. Gupta & S.S. Banarjee, Proc. Indian Science Cong., Pt. III, p. 711, 1969. 35
- [3]. “*Effect of Variation of Collector Current and Temperature on the Current Gain of the p-n-p Junction Transistor*”, R.S. Gupta & S.S. Banarjee, Proc. Indian Science Cong., Pt. III, p. 712, 1969.
- [4]. “*Characteristics of Darlington composite transistor*”, R.S. Gupta & S.S. Banerjee, Proc. Indian Science Cong., Pt. III, p. 613, 1970.
- [5]. “*Darlington Transistor Voltage Amplifier*”, R.S. Gupta & S.S. Banerjee, Proc. Indian Science Cong., Pt. III, p.613, 1970.
- [6]. “*Characteristics of Complementary Composite Transistor*”, R.S. Gupta & S.S. Banerjee, Proc. Indian Science Congr. Pt. III, p.857, 1971.
- [7]. “*Bulk semiconductor unipolar diodes - a new switching device for microwave frequencies*”, R.S. Gupta & G.S. Chilana, VI National Seminar on Semiconductor Devices (India), December 10-12, 1986.
- [8]. “*Analytical Modeling of an Ion-implanted MOSFET*”, Subhasis Haldar, Maneesha and Manoj K. Khanna & R.S. Gupta, National Seminar Workshop on System Design & Simulation, Agra April 30 to May 2, 1992.
- [9]. “*Inverse-Narrow width effect threshold voltage model of MOSFET*”, Manju Bhatia & R.S. Gupta, National Seminar Workshop on System Design & Simulation, Agra April 30 to May 2, 1992.
- [10]. “*Two Dimensional Charge Sheet Model of Short Channel MOSFET Under Non- Linear Charge Control*”, Maneesha, Subhasis Haldar, Manoj K. Khanna & R.S. Gupta, National Seminar Workshop on System Design & Simulation, Agra April 30 to May 2, 1992.
- [11]. “*New Analytical Expression for the Threshold Voltage of Short Channel IGFET*”, Manoj K. Khanna, Subhasis Haldar, Maneesha & R.S. Gupta, National Seminar workshop on system Design & Simulation, Agra April 30 to May 2, 1992.
- [12]. “*Two Dimensional I-V Model for short Channel Using a Perturbation Method*”, Rachna Sood & R.S. Gupta, Seminar on Physics and Technology of Semiconductor Devices, Pilani, 1992.
- [13]. “*An Analytical 3-D Small Geometry Effect Threshold Voltage Model of MOSFETs*”, Manju Bhatia, Rachna Sood & R.S. Gupta, Seminar on Physics & Technology of Semiconductor Devices, Pilani, 1992.

- [14]. “*GaAs MESFET Model Considering first overtone of potential*”, Rachna Sood & R.S. Gupta, National Symposium on Advances in Microwaves, New Delhi, pp. 235-244, 1993.
- [15]. “*Submicron MOSFET Threshold Voltage Model Using Non Uniformly Doped Substrate*”, Manju Bhatia & R.S. Gupta, National Symp. on Recent Advances in Microwaves, N. Delhi on March 1-2, 1993.
- [16]. “*Capacitance Calculation for non-linear Short Channel MOSFET*”, Maneesha & R.S. Gupta, National Symposium on Recent Advances in Microwave, New Delhi on March 1-2, 1993.
- [17]. “*An Analytical Modeling of Narrow Gate MOSFET*”, Subhasis Haldar & R.S. Gupta, National Symposium on Recent Advances in Microwave, New Delhi on March 1-2, 36 1993.
- [18]. “*Analytical Study of Potential Distribution and Threshold Voltage in Short Channel Fully Depleted SOI (Silicon-on-Insulator) MOSFET*”, Vaneeta Aggarwal & R.S. Gupta, National Symposium on Recent Advances in Microwaves, New Delhi on March 1-2, 1993.
- [19]. “*Effect of First Harmonic of Potential on Switching Speed of GaAs MESFETs*”, Rachna Sood, Manju Bhatia & R.S. Gupta, 18th National System Conference, Agra, pp.386-389, 1995.
- [20]. “*An improved threshold voltage model for an Ion-implanted Si MESFETs with Pearson Distribution (Type V)*”, R.S. Gupta, S. Rajesh, & Ciby Thomas, 18<sup>th</sup> National System Conference, Agra, vol. pp. 1995.
- [21]. “*Monolithic Microwave Integrated Circuit and Gallium Arsanide : A Challenge*”, R.S. Gupta, National Symposium on Recent Advance in Microwave and Light Waves 1995.
- [22]. “*Analytical Modeling of an Ion Implanted Depletion mode GaAs MESFET*”, R.S. Gupta, National Symposium on Recent Advance in Microwave and Light Waves 1995.
- [23]. “*Submicrometer lightly doped drain (LDD) MOSFET's: A device model for sub threshold regime*”, R.S. Gupta, Ciby Thomas, Y.D. Sharma an S. Haldar, National Symposium on Recent Advance in Microwave and Light Waves 1995.
- [24]. “*Two Dimensional Analytical Modeling of Drain Induced Barrier & Lowering and Sub Threshold Current Parameters for Short Channel MOSFET's*”, R.S. Gupta, Manju Bhatia and Rachna Sood, National Symposium on Recent Advance in Microwave and Light Waves 1995.
- [25]. “*Influence of pearson Distribution (FMA) on the Gate source capacitance of Si DMESFET*”, R.S. Gupta, S. Rajesh, Y.D. Sharma, National Symp. on Recent Advance in Microwave and Light Waves 1995.
- [26]. “*Analytical Modeling of Dimensional Short Channel Non-Uniformly Doped Enhancement Mode MOSFET*”, R.S. Gupta, Maneesha and S. Haldar, National Symposium on Recent Advance in Microwave and Light Waves 1995.
- [27]. “*An Improved minimum surface potential model for fully depleted SOI MOSFETs*”, R.S. Gupta and Manoj K. Pandey, National Symp. on Recent Advance in Microwave and Light Waves, 1995.

- [28]. “*An Analytical MOSFET Model with improved 2 DEG concentration*”, R.S. Gupta, Sujata Sen and Subhasis Haldar, National Symposium on Recent Advance in Microwave and Light Waves, 1995.
- [29]. “*The Effects of Pearson-IV-Distribution on Intrinsic Gate-Drain Capacitance for an Ion Implanted Si MESFET*”, R.S. Gupta, S. Rajesh, Proc. of the National Conference on Rec. Adv. in Semiconductors, New Delhi (1995).
- [30]. “*An analytical 2-D model for submicron gate GaAs MESFET*, R.S. Gupta & Sunita A. Chhokra, National Symp. on Physics of Solids and Solid State Devices, Jodhpur, Nov. 37 1996.
- [31]. “*New analytical model for non-uniformly doped short channel MOSFET from 2-D potential distributions*, R.S. Gupta, Maneesha, S. Haldar and Ciby Thomas, National Symposium on Physics of Solids and Solid State Devices, Jodhpur, November 1996.
- [32]. “*Temperature dependence of device characteristics in thin film SOI MOSFETs*”, R.S. Gupta and Prasenjeet Bose, National Symp. on Physics of Solids and Solid State Devices, Jodhpur, Nov. 1996.
- [33]. “*An analytical fringing field effect based threshold voltage model for non-uniformly doped MOSFETs*”, R.S. Gupta and Rubeena Saleem, National Symposium on Physics of Solids and Solid State Devices, Jodhpur, Nov. 1996.
- [34]. “*Modeling and Analysis of Small Geometry Depletion Mode MOSFETs*”, Subhasis Haldar, M. K Khanna, Ciby Thomas, R.S. Gupta, National Symposium on Physics of Solids and Solid State Devices, Jodhpur, November 1996.
- [35]. “*An Improved Model for Anomalous Threshold Voltage of Short Channel MOSFETs*”, Manoj K. Khanna, Ciby Thomas, S. Haldar, & R.S. Gupta, National Symposium on Physics of Solids and Solid State Devices, Jodhpur, November 1996.
- [36]. “*Above Threshold and Substrate Current Modeling of Lightly Doped Drain MOSFET (LDD)*”, Ciby Thomas, Subhasis Haldar, Manoj K. Khanna, K.K. Gupta, & R.S. Gupta, National Symposium on Physics of Solid State Devices, JNV University, Jodhpur, November 1996.
- [37]. “*A New Analytical Model for Non-Uniformly Doped Short Channel MOSFET from 2D Potential Distribution*”, Maneesha, Subhasis Haldar, Ciby Thomas, Manoj K. Khanna, and R.S. Gupta, National Symposium on Physics of Solid - State Devices, JNV University, Jodhpur, Nov. 1996.
- [38]. “*High Performance 0.1 $\mu$ m Gate Length Modulation Doped Field Effect Transistor*” Sujata Sen, Manoj K. Pandey and R.S. Gupta, Symposium on Modeling of High Frequency Transistors, Solid State Physics Laboratory, New Delhi, November 7-8, 1997.
- [39]. “*An Improved Two-Dimensional Analytical Model with Trail Function Approach for Non-Self-Aligned GaAs MESFETs*” R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, (UDSC) New Delhi, March 2-4, 1998.

- [40]. "Modelling of Fully-Depleted Double-Gate SOI MOSFET for Low-Power, High Speed VLSI Circuits", Manoj K. Pandey, Sujata Sen and R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, (UDSC) New Delhi, March 2-4, 1998.
- [41]. "A Short Channel Polycrystalline-Silicon Thin-Film Transistor for Microwave Applications", Sonia Chopra and R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, (UDSC) New Delhi, March 2-4, 1998.
- [42]. "An Improved Threshold Voltage Model for Short Channel Non-Uniformly Doped Channel (NUDC) MOSFETs" Rubeena Saleem, Srikanta Bose and R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, (UDSC) New Delhi, March 2-4, 1998.
- [43]. "Influence of DX Center on 2-DEG Modelling of LM-HEMT", Sujata Sen, Manoj K. Pandey and R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, (UDSC) New Delhi, March 2-4, 1998.
- [44]. "Modelling of Hot Carrier Immunized Short Geometry LDD MOSFET Considering DIBL Effect", Ekta Kalra, Anil Kumar, Subhasis Halder and R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, (UDSC) New Delhi, March 2-4, 1998.
- [45]. "Temperature Dependence and Scattering Mechanism Effect on the Electron Mobility and  $I_d - V_d$  Characteristics of GaAs MESFET", Srikanta Bose, Rubeena Saleem and R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, (UDSC) New Delhi, March 2-4, 1998.
- [46]. "A unified model for flicker and white noise of small geometry lightly doped drain MOSFET", Ekta Kalra, Anil Kumar, Subhasis Halder and R.S. Gupta, National Seminar Applied Systems Engineering & Soft Computing (SASESC-2000), Agra, in March 4-5, 2000.
- [47]. "Unified MOSFET model including reverse short channel and narrow width effects for device modelling in circuit simulation", Anisha Goswami, Anju Agarwal and R.S. Gupta, National Seminar Applied Systems Engineering & Soft Computing (SASESC- 2000), Agra, March 4-5, 2000.
- [48]. "Analytical study of short channel GaAs OPFET" Srikanta Bose, Mridula Gupta, and R.S. Gupta, National Seminar Applied Systems Engineering and Soft Computing (SASESC-2000), Agra, in March 4-5, 2000.
- [49]. "A two dimensional threshold voltage of small geometry poly-Si TFT", Sonia Chopra and R.S. Gupta, National Seminar Applied Systems Engineering and Soft Computing (SASESC-2000), Agra, in March 4-5, 2000.
- [50]. "A resistance based noise model fo fully overlapped lightly doped drain MOSFET" A Kumar, E Kalra, S Halder and R S Gupta, National Seminar Applied Systems Engineering and Soft Computing (SASESC-2000), Agra, in March 4-5, 2000.
- [51]. "An analytical model for current-voltage characteristics of GaN/AlGaIn-doped channel HEMT", Rashmi, Sujata Sen, Subhasis Halder and R S Gupta, National Seminar Applied Systems Engineering and Soft Computing (SASESC-2000), Agra, in March 4-5, 2000.

- [52]. "A new quasi-2d short channel model for I-V characteristics of fully depleted thin film surrounded/cylindrical gate MOSFET", Abhinav Kranti, S Haldar and R S Gupta, National Seminar Applied Systems Engineering and Soft Computing (SASESC-2000), Agra, in March 4-5, 2000.
- [53]. "Two dimensional charge control model for pseudomorphic (AlGaAs/InGaAs) modulation doped field effect transistor", Anju Agarwal, Anisha Goswami and R S Gupta, National Symposium on Advance in Microwave and Lightwaves, March 25- 28, 2000, New Delhi.
- [54]. "An analytical  $I_{ds}$ - $V_{ds}$  model for AlGa<sub>N</sub>/Ga<sub>N</sub> MODFET", Rashmi, Sujata Sen, Subhasis Haldar and R S Gupta, National Symposium on Advance in Microwave and Lightwaves, March 25-28, 2000, New Delhi.
- [55]. "A new analytical model for current-voltage characteristics of InAlAs/InGaAs High electron mobility Transistor", Joytika Jogi, Srikanta Bose, Sujata Sen, Mridula Gupta and R S Gupta, National Sympo. on Advance in Microwave & Lightwaves, March 25-28, 2000, New Delhi.
- [56]. "Low frequency  $1/f$  noise of fully overlapped lightly doped drain MOSFET", Anil Kumar, Ekta Kalra, Subhasis Haldar and R S Gupta, National Symposium on Advance in Microwave and Lightwaves, March 25-28, 2000, New Delhi.
- [57]. "An analytical model of potential distribution and threshold voltage for thin film fully depleted surrounding gate (FD-SGT) MOSFET", Abhinav Kranti, Subhasis Haldar & R S Gupta, National Symposium on Advance in Microwave and Lightwaves, March 25-28, 2000, New Delhi.
- [58]. "Noise modelling of small geometry lightly doped MOSFET", Ekta Kalra, Anil Kumar, Subhasis Haldar and R S Gupta, National Symposium on Advance in Microwave and Lightwaves, March 25-28, 2000, New Delhi.
- [59]. "Admittance parameters extraction for MOSFET valid upto 10 GHz", Anisha Goswami, Anju Agarwal, Mridula Gupta and R S Gupta, National Symposium on Advance in Microwave and Lightwaves, March 25-28, 2000, New Delhi.
- [60]. "Analytical model for threshold voltage adjustment by gate workfunction control in double gate SOI MOSFETs", Abhinav Kranti, Ritesh Gupta, S Haldar and R S Gupta, In Proceedings National seminar on VLSI: Systems, Design & Technology, IIT Bombay, 2000.
- [61]. "An accurate charge control model for InAlAs/InGaAs/InP modulation doped field effect transistors", Ritesh Gupta, Abhinav Kranti, S Haldar, Mridula Gupta and R S Gupta, Proceedings of Symposium on Advances in Electronics (ELECTRO-2001) January 4-6, 2001, BHU, Varanasi.
- [62]. "An analytical 2-dimensional model for AlGa<sub>N</sub>/Ga<sub>N</sub> modulation doped field effect transistor (MODFET)", Rashmi, S Haldar and R S Gupta, Proceedings of Symposium on Advances in Electronics (ELECTRO-2001) January 4-6, 2001, BHU, Varanasi.
- [63]. "An analytical model for I-V characteristics of optically controlled surrounding/cylindrical gate (SGT) MOSFET", Abhinav Kranti, Ritesh Gupta, S Haldar and R S Gupta, Proceedings of Symposium on Advances in Electronics (ELECTRO-2001) Jan. 4-6, 2001, BHU, Varanasi.

- [64]. “*Microwave performance of pseudomorphic modulation doped field effect transistor (AlGaAs/InGaAs) for millimeter wave and high speed circuit applications*”, Anju Agarwal and R S Gupta, Proceedings of Symposium on Advances in Electronics (ELECTRO-2001) January 4-6, 2001, BHU, Varanasi.
- [65]. “*Complete analysis of polysilicon TFT using charge sheet approach*” Simrata Bindra, Subhasis Haldar and R.S. Gupta, National Conference on Recent Advances in Microwaves, Antennas and Propagation, November 2-4, 2001, Jaipur.
- [66]. “*A new analytical model of partially relaxed Al<sub>m</sub>Ga<sub>1-m</sub>N/GaN high electron mobility transistors for microwave applications*” Rashmi, Abhinav Kranti and R.S. Gupta, National Conference on Recent Advances in Microwaves, Antennas & Propagation, Nov. 2- 4, 2001, Jaipur.
- [67]. “*An analytical approach to characterize microwave performance of vertical surrounding gate (VSG) MOSFETs*”, Abhinav Kranti, Rashmi and R.S. Gupta, National Conference on Recent Advances in Microwaves, Antennas and Propagation, November 2-4, 2001, Jaipur.
- [68]. “*Temperature Dependent Electrical Characteristics of Short Geometry Poly Si TFT for High Frequency Applications*” Amit Sehgal, Tina Mangla, Mridula Gupta and R. S. Gupta, INCURSI-2003, November 27 – 29, 2003, NPL, New Delhi.
- [69]. “*A Physics based Numerical Model of Nonuniformly Doped Channel 6H-Silicon Carbide MOSFET*” Navneet Kaushik, Subhasis Haldar, Mridula Gupta and R.S. Gupta, INCURSI-2003, November 27 – 29, 2003, NPL, New Delhi.
- [70]. “*A Lattice Temperature Dependent Thermal Noise Model For Fully Depleted SOI MOSFET*” Nirupma Kapoor, Subhasis Haldar, Mridula Gupta and R.S. Gupta, National Symposium on Advances in Microwave and Lightwave, 13 – 14th October 2003, UDSC, New Delhi.
- [71]. “*Temperature Dependent Threshold Voltage modeling of short geometry Poly Si TFT*” Amit Sehgal, Tina Mangla, Mridula Gupta and R. S. Gupta, National Symposium on Advances in Microwave & Lightwave, 13–14th Oct. 2003, UDSC, New Delhi.
- [72]. “*Depletion dependent analytical model for InAlAs/InGaAs/InP HEMT*” Ritesh Gupta, Tina Mangla, Sandeep Aggarwal, Mridula Gupta and R.S. Gupta, National Symposium on Advances in Microwave and Lightwaves, October 13- 14, 2003, Pp. 52- 55. UDSC, New Delhi.
- [73]. “*Two-Dimensional Analytical Threshold Voltage Model for Dual Material Gate (DMG) Epi-MOSFET,*” Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, National Conference on VLSI Design & Technology, Bharti Vidyapeeth’s College of Engineering, New Delhi, April 15-16, p.35, 2004.
- [74]. “*Two-dimensional analytical modeling and simulation of a novel structure triplematerial gate stack (TRIMAGAS) MOSFET*”, R.S. Gupta, Kirti Goel, Manoj Saxena and Mridula Gupta, Proceedings of Symposium on Emerging Trends in Electronics (ELECTRO-2005) Page 134-137, February. 3-5, 2005, BHU, Varanasi.

[75]. “*Two-Dimensional Analytical Modeling and Simulation of Multiple Material Gate Oxide Stacked MOSFET*,” Kirti Goel, Manoj Saxena, Mridula Gupta and R.S. Gupta, National Conference on Integrated Broad Band Digital Systems and Networks, NIEC, Delhi, March 18-19, 2005.

[76]. “*RF Performance Investigation of Gate Stacked Insulated Shallow Extension (ISE) MOSFET and Bulk: A Comparative Study*,” Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R. S. Gupta, National Conference on Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2006), pp 254-258, 24-26 March 2006, New Delhi, India.

[77]. “*An analysis of Bias Dependent Performance of AlGa<sub>N</sub>/Ga<sub>N</sub> Modulation Doped Field Effect Transistor Using Accurate Velocity-Field Dependence*”, Sona P. Kumar, Anju Agrawal, Sneha Kabra, Mridula Gupta and R.S. Gupta, National Conference on Mathematical Techniques Emerging Paradigm for Electronics and IT Industries (MATEIT 2006), pp 254-258, 24-26 March 2006, New Delhi, India.

[78]. “*An analytical two dimensional threshold voltage model for sub-micron Ga<sub>N</sub> MESFET*” Sneha Kabra, Harsupreet Kaur, Subhasis Haldar, Mridula Gupta, and R. S. Gupta, National Conference on Recent Advancements in Microwave Technique and Applications (Microwave - 2006) Jaipur, October 6 - 8, 2006.

[79]. “*Bias dependent analytical model of AlGa<sub>N</sub>/Ga<sub>N</sub> high electron mobility transistor*” Sona P Kumar, Anju Agrawal, Sneha Kabra, Mridula Gupta and R.S. Gupta, National Conference on Recent Advancements in Microwave Technique and Applications (Microwave -2006) Jaipur, October 6 - 8, 2006.

[80]. “*An analytical drain current model for graded channel fully depleted cylindrical / surrounding gate MOSFET*” Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S. Gupta, National Conference on Recent Advancements in Microwave Technique and Applications (Microwave -2006) Jaipur, October 6 - 8, 2006.

[81]. “*Lateral channel engineered structure- Insulated shallow extension (ISE) MOSFET: DC and RF performance investigation*” Ravneet Kaur, Rishu Chaujar, Manoj Saxena, R. S. Gupta, National Conference on Recent Advancements in Microwave Technique and Applications (Microwave -2006) Jaipur, October 6 - 8, 2006

[82]. “*Exploring the effect of negative junction depth on electrical behaviour of sub-50-nanometer concave DMG MOSFET: A simulation study*” Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R. S. Gupta, National Conference on Recent Advancements in Microwave Technique and Applications (Microwave -2006), Jaipur, October 6 - 8, 2006

[83]. “*New concave MOSFET with transverse dual material gate (T-DMG) in sub-50nm regime: A simulation study*” Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, Indian Microelectronics Society Conference, 2007, Punjab Engineering College, Chandigarh, August 17 – 18, 2007.

[84]. “*Effect of transport property on the performance of insulated shallow extension gate stack (ISEGaS) MOSFET*” Ravneet Kaur, Rishu Chaujar, Manoj Saxena and R.S. Gupta, Indian

Microelectronics Society Conference, 2007, Punjab Engineering College, Chandigarh, August 17 – 18, 2007.

[85]. “*Modeling issues of heterojunction transistor for very large scale integrated (VLSI) applications*” Parvesh, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R.S. Gupta, Indian Microelectronics Society Conference, 2007, Punjab Engineering College, Chandigarh, August 17 – 18, 2007.

[86]. “*A 2-D analytical model for gate misalignment effects on graded channel DG FD SOI n-MOSFET*”, Rupendra Kumar Sharma, Manoj Saxena, Mridula Gupta and R.S. Gupta, Indian Microelectronics Society Conference, 2007, Punjab Engineering College, Chandigarh, August 17 – 18, 2007.

[87]. “*Graded channel (CG) design in surrounding gate MOSFET (SGT) for improving short channel and hot carrier performance*” Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S. Gupta, Indian Microelectronics Society Conference, 2007, Punjab Engineering College, Chandigarh, August 17 – 18, 2007.

[88]. “*Simulation of a Novel ISE MOSFET with Gate Stack Configuration*”, R. Kaur, R. Chaujar, R. S. Gupta and M. Saxena, The Second National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[89]. “*Development Board-Level Experimentation and Simulation of FPGA based DEBPSK DSSS Modulator: Implementation of 10-Chip Gold Code Sequence Generator*”, Rishu Chaujar, Ravneet Kaur, Manoj Saxena, Mridula Gupta and R.S. Gupta, The Second National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[90]. “*A Two-Dimensional Threshold Voltage Model for Asymmetric Gate Stack Surrounding Gate MOSFET*”, Harsupreet Kaur, Sneha Kabra, Subhasis Haldar and R.S. Gupta, The Second National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[91]. “*Impact of Dual Material Gate Design on AlGaIn/GaN High Electron Mobility Transistor's RF Performance*”, S. P. Kumar, A. Agrawal, R. Chaujar, M. Gupta and R. S. Gupta, The Second National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[92]. “*Theory of Charge Control Characteristics of AlGaIn/GaN MISHFET: A High Temperature Study*”, Ruchika Aggarwal, Anju Agrawal, Mridula Gupta and R.S. Gupta, The Second National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[93]. “*High Temperature Performance of AlGaIn/GaN HEMT*”, Parvesh, Ravneet kaur, Sujata Pandey, Subhasis Haldar, Mridula Gupta and R S Gupta, The Second National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[94]. “*Effect of Control Gate Length on Device Performance of GMETRC MOSFET*”, Priyanka Malik, Rishu Chaujar, Sona P. Kumar, Mridula Gupta and R.S. Gupta, The Second National



Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[95]. “Analytical Modeling of Multi-Layered Dielectric G4-MOSFET for Improved Short Channel Effects”, N. Sharma, J. Bansal, S. P. Kumar, R. Chaujar, M. Gupta and R.S. Gupta, The Second National Conference on Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2008), New Delhi, September 26-28, 2008.

[96] “Effect of technology parameter variation on RF Performance for Gate Material Engineered-Trapezoidal Recessed Channel (GME-TRC) MOSFET”, Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S.Gupta, MATEIT - 2010, 3rd National Conference on Mathematical Techniques : Emerging Paradigms for Electronics and IT Industries, January, 30-31, 2010.

[97] “Impact Of Localised Charges On The Device Reliability Of The Silicon Nanoscale Surrounding Gate Mosfet”, Rajni Gautam, Manoj Saxena, R.S.Gupta and Mridula Gupta, National Conference and Workshop On Recent Advances in Modern Communication Systems and Nanotechnology (NCMCN- 2011), 6th -8th Jan. 2011, Jaipur, India.

[98] “Effect of temperature variation on various parameters in Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET: A Simulation Study” Vandana Kumari, Manoj Saxena, R.S.Gupta and Mridula Gupta. National Conference and Workshop On Recent Advances in Modern Communication Systems and Nanotechnology (NCMCN- 2011), 6th -8th Jan. 2011, Jaipur, India.

[99] “Performance Comparison of Silicon and SiGe based Double Gate Tunneling Field Effect Transistor with gate stack architecture”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta. National Conference and Workshop On Recent Advances in Modern Communication Systems and Nanotechnology (NCMCN- 2011), 6th -8th Jan. 2011, Jaipur, India.

[100]. “Impact of Insulating Layers on Single and Double Gate MOSFET for Improved Short Channel Effect and Hot Carrier Reliability”, Vandana Kumari, Manoj Saxena, R.S. Gupta, and Mridula Gupta, NCRDE 2013, University of Delhi 18-20 January, 2013.

[101]. “Gate Length and Donor –Layer Characteristic Optimization of InAlAs/InGaAs DG-HEMT for improved RF and Noise Performance” Monika Bhattacharya, Jyotika Jogi, R.S Gupta and Mridula Gupta, NCRDE 2013, University of Delhi 18-20 January, 2013.

[102]. “Analytical I-V Model for Dual Metal Gate Surrounding MOSFET”, Pujarini Ghosh, Subhasis Haldar, R.S Gupta and Mridula Gupta, NCRDE 2013, University of Delhi 18-20 January, 2013.

[103]. “Performance Investigation of Silicon Nanowire Tunnel FET for Analog and Digital Application”, Rakhi Narang, Manoj Saxena, R. S. Gupta and Mridula Gupta, NCRDE 2013, University of Delhi 18-20 January, 2013.

[104]. “Surface Potential model of Triple material Gate Graded Channel Gate Stack Surrounding Gate (TMG-GC-GS SCT) MOSFET”, Jay Hind Verma, Yogesh Pratap, Subhasis Haldar, R.S Gupta and Mridula Gupta, NCRDE 2013, University of Delhi 18-20 January, 2013.

[105]. “High Performance Low Power 6T RAM Cell Using Gate-All Around (GAA) MOSFET”, Rajni Gautam, Manoj Saxena, R.S.Gupta, and Mridula Gupta, NCRDE 2013, University of Delhi 18-20 January, 2013.