

Mr. Praween Kumar

Designation: Assistant Professor

Qualification: Ph.D. (Purs.), M.Tech., AMIETE, B.Sc Phy(Hons.)

Specialization: VLSI, Analog Signal Processing, VHDL

Email Id: pksinha@mait.ac.in

Office Address: Room No. 413, 4th Block, MAIT, Sec – 22, Rohini, Delhi – 86



Education

Ph. D. (Purs) in Realization of Active Network for Instrumentation & Communication.

M. Tech. in Electronic Design & Technology from Gorakhpur University, 2002.

Bachelors (AMIETE) in Electronics & Communication from IETE, 2000

B.Sc Phy (Hons.) from Bhagalpur University 1995

Special Achievements:

Best Teacher Award for the session 2007-08 in MAIT

Research Interest

Analog Signal Processing, Low Power CMOS.

Publications

International Journals: 06

National Journals: 03

International Conferences: 0

National Conferences: 01

Selected Papers

[1]. Praween Kumar Sinha, Neelam Sharma, Rohit Mishra “A Configuration for Realizing Voltage Controlled Floating Inductance and Its Application” Circuit & Systems Scientific Research Publications (USA), Vol 6, PP 189-199, 2015.

[2]. Praween Kumar Sinha, Neelam Sharma, Simran Agarwal, Sudipto Saha “CFOA BASED BANDPASS AND BANDSTOP LADDER FILTER-A NEW CONFIGURATION” Circuit & Systems Scientific Research Publications (USA), Vol 7, PP 29-42, 2016.

[3]. Praween K. Sinha, Akshay Saini, Pranav Kumar, Sumit Mishra “ CFOA Based Low Pass and High Pass Ladder Filter – A new configuration” circuit and systems Scientific Research Publications (USA), Vol 5, PP 293-300, 2014,.

[4]. Praween kumar sinha, Ramakanta chaudhary and umakanta chaudhary “Design of current Mirror and temperature Effect with compensation technique” JAPED (USA); Vol8, number 2-3 P 219-229, (2013).

[5]. Praween sinha, Ajay Shankar, Mohit Arora and Mohit Datta “Design and implementation of Low Volume, High Bandwidth MOS current Mirrors”, JAPED (USA) vol8, Number (2-3) P 239-251, (2013).

[6]. Praween kukmar Sinha “systematic approach for Implementing controlled source’s using current feedback operational Amplifiers”, JAPED (USA) Vol 9, number (2-3), P 115-131, (2014).

Books Published

[1]. VLSI Design in Typing Stage