Prof. (Dr.) Neelam Sharma

Designation: HOD ECE

Qualification: Ph.D. , M.Tech., B.Tech.

Specialization: VLSI Technology, VLSI Design, Computer Architecture, Digital Logic Design, Microprocessor & Microcontroller

Email Id: **neelam_sr@yahoo.com** **;** maithodece@gmail.com

Office Address: Room No. 413, 4TH Block, MAIT, Sec – 22, Rohini, Delhi – 86

Education

Ph. D. in Development of Fast VLSI RBSD Pipelined Arithmetic Logic Unit from UPTU Lucknow ,2006.

Masters in M.Tech. (Digital Systems branch from, UPTU Lucknow , 2002

Bachelors in B.Tech (EC) Hons from Thapar Institute of Engineering & Technology Patiala, Punjab , 1985

Gold Medal for Pre-Engg. Examination(XII), GND University.

(3rd Position in B.Tech. at Thapar Institute of Engeering & Technology.

Awarded Best Girl in School (Loreto Convent, Lucknow) 1979.

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Research Interest

VLSI Technology, VLSI Design, Computer Architecture, Digital Logic Design, Bio-Medical Electronics.

Publications

International Journals: 20

National Journals: 00

International Conferences: 26

National Conferences: 17

Total Publications: 63

Selected Papers

1. **Neelam Sharma**, B.S. Rai and Arun Kumar, "Design of RBSD Adder and Multiplier Circuits for High Speed Arithmetic Operations and their Timing Analysis " A Gelbukh, S. Suarez.(Eds.) received 24/06/2006. International Journals from Centre for computing research. Mexico city, Russia.
2. **Neelam Sharma**, B.S. Rai and Arun Kumar, "Design of RBSD Adder and Multiplier Circuits for High Speed Arithmetic Operations and their Timing Analysis" Advances in Computer Science and Engineering. Accepted 07/10/2006. International Journals from Centre for computing research. Mexico city, Russia.
3. **Neelam Sharma**, Rakesh Saxena and A.K. Wadhwani "Novel Design of Fast RBSD Adder with Reduced NOR – NOR Logic", **International Journal of Computer and Network Security** (**IJCNS)** Vol.2 No.7 July 2010 **Austria, Vienna.**
4. **Neelam Sharma**, Reena Rani, Upasana Agrawal, Laxmi Kant Singh, **"**High Speed Arithmetic Logical Unit using Quaternary Signed Digit Number System" **International Journal of Electronics Engineering, IJEER.** ISSN 0975 – 6450 Volume 2 Number 3 (2010) pp. 383 – 391. website http://www.ripublication.com/ijeer.htm
5. Rakesh Kumar Saxena, **N. Sharma**, A. K. Wadhwani, "FPGA Implementation of fast redundant adder using universal logic" Published in the Journal of Indian Society of Industrial and Applied Mathemetics, Special issue of July 2011.
6. Rakesh Kumar Saxena, **Neelam Sharma,** A. K Wadhwani, "Design of Fast Pipelined Multiplier using Modified Redundant Adder", International Journal of Intelligent Systems and Applications (IJISA), **MECS Publisher Hongkong .**
7. Rakesh Kr. Saxena, **Neelam Sharma** and A.K. Wadhawani "Fast Adder Design using Relevant Binary Numbers with Reduced Chip Complexity" International journal of Engineering and Technology, Vol. No. – 3, 3rd June – 2011.
8. Rakesh Kumar Saxena, **Neelam Sharma**, A.K Wadhwani "Performance Analysis of Various Universal Logic Redentant Adders" International journal of Engineering Research & Technology (IJERT), Aug., 2015.
9. **Neelam Sharma**, Reena Rani and L.K. Singh, "FPGA Implementation of Fast Adders using Quaternary Signed Digit Number System", **IEEE Explorer** 2010. International Conference on Emerging Trends in Electronic and Photonic Devices & Systems - Dec 2009 at IT – BHU, Varanasi.
10. **Neelam Sharma**, Reena Rani and L.K. Singh, "Fast Computing using Signed Digit Number System", **IEEE Explorer** 2009.
11. R.K. Saxena, **Neelam Sharma** and A.K. Wadhwani, "Fast Arithmetic using Signed Digit Numbers and Ternary Logic", Proceedings of International Conference held at American Institute of Physics, USA., 14-16 Jan. 2009.

Books Published

[1] **Dr. Neelam Sharma** "Basic Electrical & Electronics Engineering" Published by Ashirwad Publications, Third Edition 2014-15

[2] **Dr. Neelam Sharma,** Dr. Anil Sharma and Ms. Neha Singh, "Digital Logic Design" published by the "Ashirwad Publications, Jaipur (Raj.)" First Edition – July 2011-12.

[3] **Dr. Neelam Sharma,** Dr. Anil Sharma and Ms. Neha Singh edited the book titled "Basic Electrical & Electronics Engineering" published by the "Ashirwad Publications, Jaipur (Raj.)" First Edition - Aug. 2011-12.

[4] **Dr. Neelam Sharma,** Dr. Anil Kr. Sharma and Ms. Neha Singh "B.Tech Solved Papers – I Sem" published by Ashirwad Publications, Jaipur (Raj.)" First Edition - 2012-13 (ISBN No. – 978-93-80343-83-9)

[5] **Dr. Neelam Sharma,** Chief Editor of Souvenir for Seminar on Global Trends in Technology and Industry : Impact on and Society published by Delhi Technical Campus, G. Noida

[6] **Dr. Neelam Sharma,** Edited the International Conference Proceedings on Global Trends in Technology: Impact on Industry and Society (IGTT-11) published by Institute of Engineering and Technology, Alwar, Raj. India. Oct. 2011.

Sponsored Projects:

[1]. **AICTE Grant: Received AICTE project grants** worth 90.00 Lacs for SDP, MODROBS and RPS Schemes for I.E.T.,Alwar (Raj).

[2]. **World Bank Grant:** Institute of Engineering & Technology, Alwar was selected under TEQIP Phase – II subcomponent 1.1 from NPIU Noida for **fund of Rs. 4.00 Cr**.on the basis of report prepared by me as a Principal of the organization (I.E.T.,Alwar (Raj)).The fund was released to the Institute for up-gradation of Faculty, students & Labs.

Ph. D. Thesis Guided: 05 Students (01 Awarded, 01 Submitted, 03 Registered)

M.Tech.Dissertation Guided : 18

B.Tech Projects Guided:. 45

Professional Membership: Member IETE, IEEE, IE, CSI.

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