# Ms. Sumedha Gupta

**Designation:** Assistant Professor

**Qualification:** Ph.D (Purs.), M.Tech, B.Tech

**Specialization:** VLSI Design and Modeling of Microelectronic Devices

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## *Education*

Ph.D. (Pursuing) from Delhi Technological University.

M.Tech in Signal Processing from GGSIPU, 2011-2013.

B.Tech in Electronics and Communication Engineering from GGSIPU, 2007-2011.

## *Research Interest*

VLSI Design, Semiconductors, Modeling and Design

## *Publications*

International Journals: 02
International Conferences: 02

## *List of Publications*

[1]. Gupta, S., Pandey, N., & Gupta, R. S. (2020, December). Investigation of dual-material double gate junctionless accumulation-mode cylindrical gate all around (dmdg-jlam-cgaa) mosfet with high-k gate stack for low power digital applications. In *2020 IEEE 17th India council international conference (INDICON)* (pp. 1-4). IEEE.

[2]. Gupta, S., Pandey, N., & Gupta, R. S. (2021). Analytical modeling of dual-metal gate stack engineered junctionless accumulation-mode cylindrical surrounding gate (DMGSE-JAM-CSG) MOSFET. *Applied Physics A*, *127*(7), 1-10.

[3]. Gupta, S., Pandey, N., & Gupta, R. S. (2021, May). Analog Performance of Dual-Metal Gate Stack Architecture of Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSA-JAM-CSG) MOSFET. In *2021 Devices for Integrated Circuit (DevIC)* (pp. 1-5). IEEE.

[4]. Gupta, S., Pandey, N., & Gupta, R. S. (2021). Temperature dependency and linearity assessment of dual-metal gate stack junctionless accumulation-mode cylindrical surrounding gate (DMGS-JAM-CSG) MOSFET. *Physica Scripta*, *96*(12), 124055.