About MAIT

Maharaja Agrasen Institute of Technology an ISO 9001:2015 certified Institute, was established in 1999 by Maharaja Agrasen Technical Education Society promoted by a group of well known Industrialists, Businessman, Professionals and Philanthropists with an aim to promote quality education in the field of Technology and Management. Since then, MAIT has grown from strength to strength to emerge as one of the top technical institutes among the private Institutes with three NBA accredited programmes (CSE, ECE and MAE).

The Vision of Institute is to nurture young minds in a learning environment of high academic value and imbibe spiritual and ethical values with technological and management competence.

The Vision of ECE Department is to excel in technical education and provide a valuable resource to Electronics industry and society. The department is committed to promote effective teaching, inculcate creative thinking and to develop a strong centre of Excellence.

Course Contents

Evolution of electronics & VLSI Design. Very large scale integration – Monolithic and Hybrid IC, VLSI Design isolation, Oxide isolation, Diode Isolation, Building blocks, Layout of Passive element. Resistor geometry, Power dissipation, Power density, Tolerance. Design of semiconductor diffused resistors, thin film resistor and Monolithic Capacitor. Fabrication of thick oxide MOSFET and CMOS. Design of Silicon Integrated circuits, Concept of buried layer, Initial Artwork, Isolation Diffusion. Analytical modeling of MOS Devices in VLSI, Deep sub-micron modeling, Advance MOSFET Design Structure. CMOS Digital IC Design, Threshold Voltage of Digital IC, InverterDesign.

Course Faculty:

1. Prof. R.S. Gupta
2. Dr. Yogesh Pratap
3. Dr. Manoj Kumar

Lab Faculty:

1. Dr. Praween Sinha
2. Dr. Sonam Rewari
3. Mr. Nitin Trivedi

Industry Experts:

1. Mr. Mayank Singh (CoreEL)
2. Mr. Ankur Singhal (CoreEL)

One-Week
FACULTY DEVELOPMENT PROGRAM

on

VLSI Design and Modeling

(Intensive Short Course)

6th May. 2019 to 11th May 2019

Organized by:

Department of Electronics and Communication Engineering
Maharaja Agrasen Institute of Technology

Sponsored by:

Society of Microelectronics & VLSI
And
IEEE – EDS Delhi Chapter

Venue :

Seminar Hall Room 401A
& VLSI Design and Modeling Lab
[422]/ [402(B)]
Maharaja Agrasen Institute of Technology
Sector 22 Rohini
New Delhi – 110086
(www.ece.mait.ac.in)

Time: 10:00 A.M. – 4:00 P.M.

Chief Patron

Dr. Nand Kishore Garg
Founder Chairman and Chief Advisor, MATES
Chancellor, MAU,HP

Shri Prem Sagar Goel
Chairman,MATES, Delhi

Patron

Prof. (Dr.) M. L. Goyal
Vice Chairman (Academics), MATES, Delhi

Director, MAIT

Prof. (Dr.) Neelam Sharma

Head – ECE Department

Prof. (Dr.) Sunil Kumar

Contact Details

For more details, please contact:

Dr. Praween Kumar
Email: pksinha@mait.ac.in
Mobile: 9953285212

Mr. Vaibhav Nijhawan
Email: vaibhavnijhawan@mait.ac.in
Mobile: 9811556771

Registration Form

Registration Fee: Rs. 1000.00

Mode of payment:

1. **NEFT: Account No. : 394502010059875**
   IFSC Code : UBIN0560421
2. **PAYTM Number : 8448186940**
3. **Cash (At Registration desk)**

Dr. / Mr. / Ms.: _____

Designation: _____

Organization: _____

Experience: _____

Mobile: _____

E-mail: _____

Transaction Id: _____

Declaration

The information furnished above is true to the best of my knowledge. I agree to abide by the rules and regulations governing the FDP.

Place:

Date:

Signature of Applicant:

Local Hospitality

Registered participants will be provided with free registration kit, lunch, snacks and tea/ coffee at the venue.

Registration of Participants

The interested faculty members of the different colleges may register themselves by filling the registration form (attached) duly attested by concerned Head of the Institution / Head of the Department and thereafter sending the scanned copy (in jpeg format) at any of the e-mail IDs mentioned in the contact details.

- *Limited Seats are available.*
- *Selection of participants shall be done on first come first serve basis*
- *Participants need to bring the original copy of the registration form as well as their college identity card at the time of FDP*
- *Certificate of participation will be provided by Department of ECE, MAIT.*

Important Dates

Dates of FDP
6th May. 2019 to 11th May 2019

Last date of registration
2th May. 2019

Notification of Selection
4th May. 2019